

MS-7A38 Ver:5.0

CPU:
AMD AM4

System Chipset:
Promontory B350/A320
(Value DIY or System Builder)

Main Memory:
DDR IV * 4 MAX:64 GB

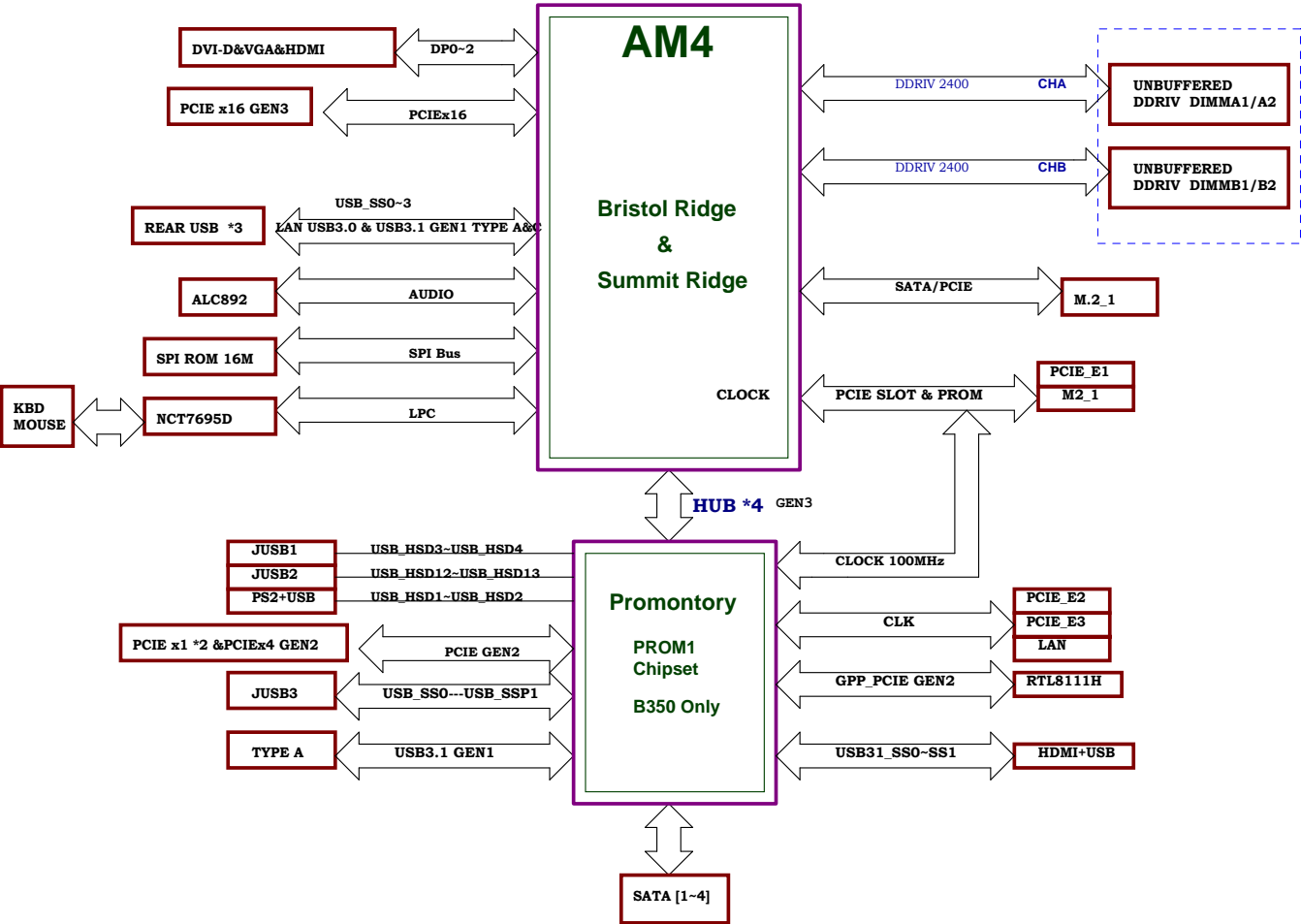
VRM
RT8894 4+2

On Board Chipset:
LPC Super I/O --NCT6795D
LAN RTL8111H
Azalia CODEC - Realtek ALC887

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1

OCF IC:
UP6273

FUSION BLOCK DIAGRAM

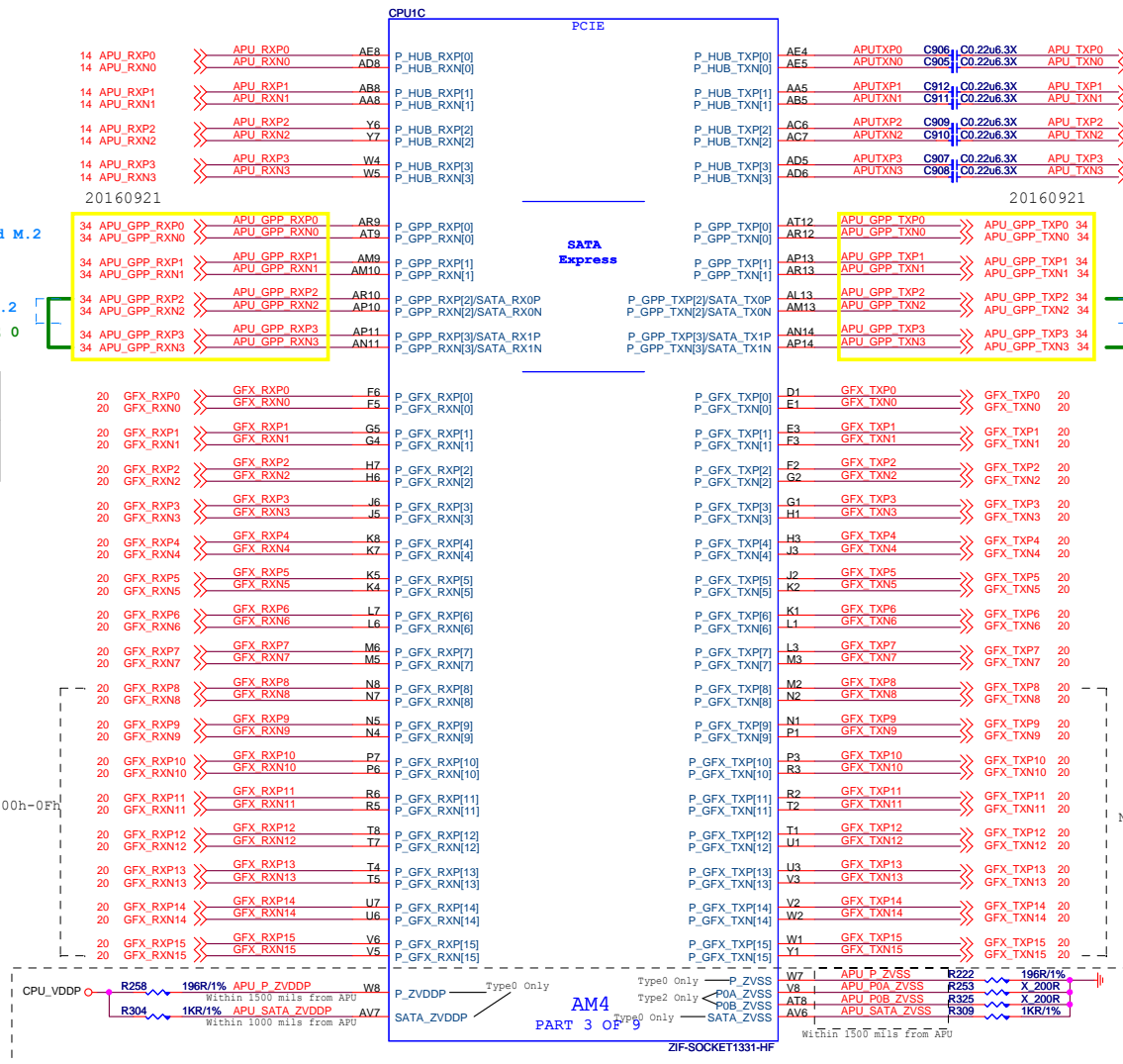


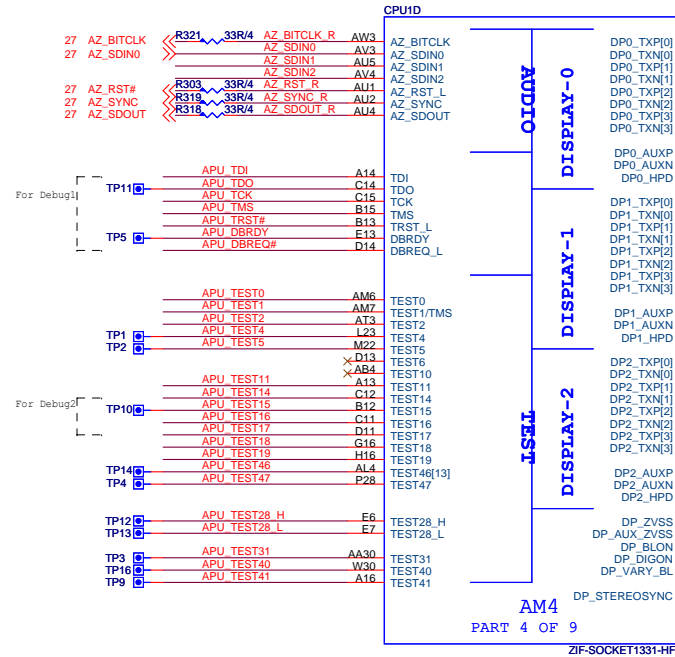
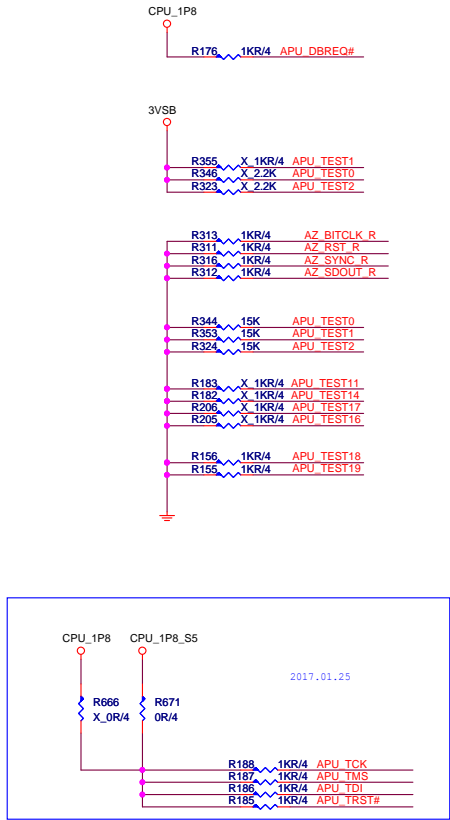
AMD AM4

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04 AM4 PCIE/SATAE	40 PM-NB681-1.05V/GS7133-2.5V
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06 AM4 SVI/ACPI/GPIO	42 DDR4 8125E Power
07 AM4 LPC/SPI/USB/CLK/STRAP	43 CPU Power 1P8V-MP2147
08 AM4 Power/RTC Power/ 09 AM4 GND	44 CPU Power VDDP-RT8125E
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32 USB Rear HDMI+TYPE A	
33 USB Front Side	
34 M.2	
35 SATA Connector	
36 DP to VGA ITE6516	

	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

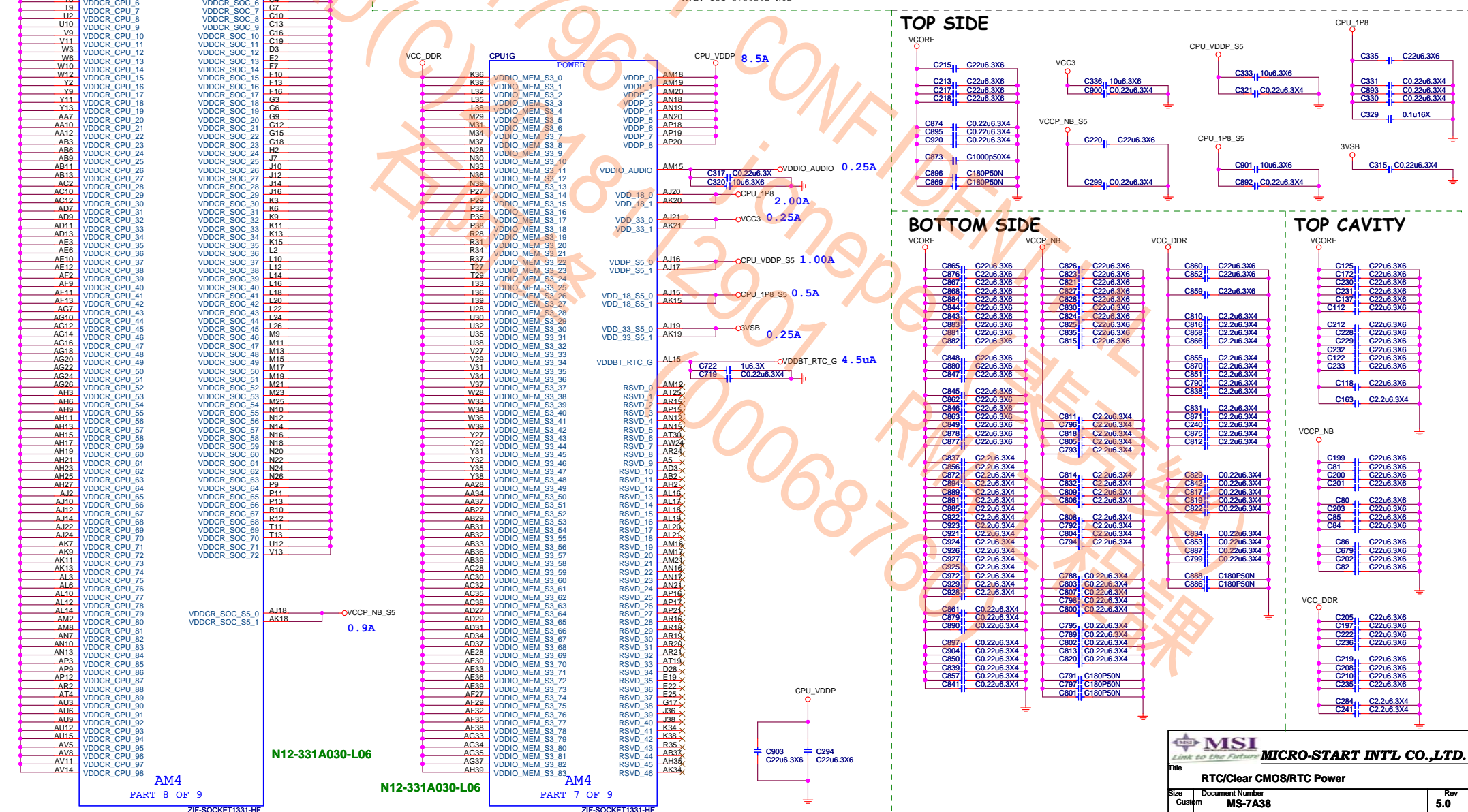
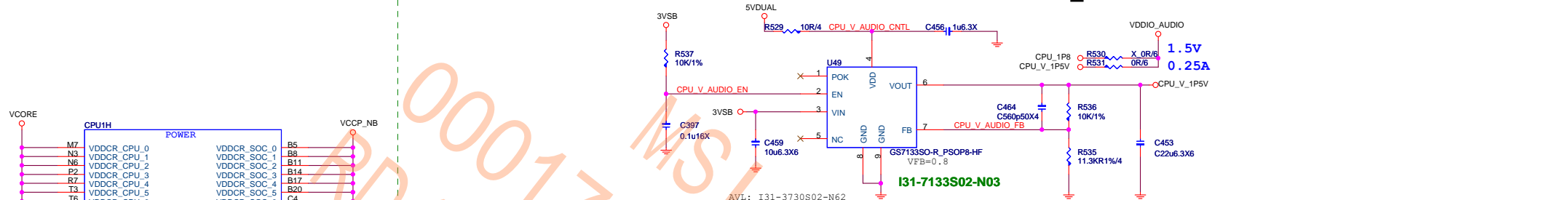
Only supported on AMD Family 17h/Models 00h-0Fh





N12-331A030-L06

VDDIO_AUDIO Circuit

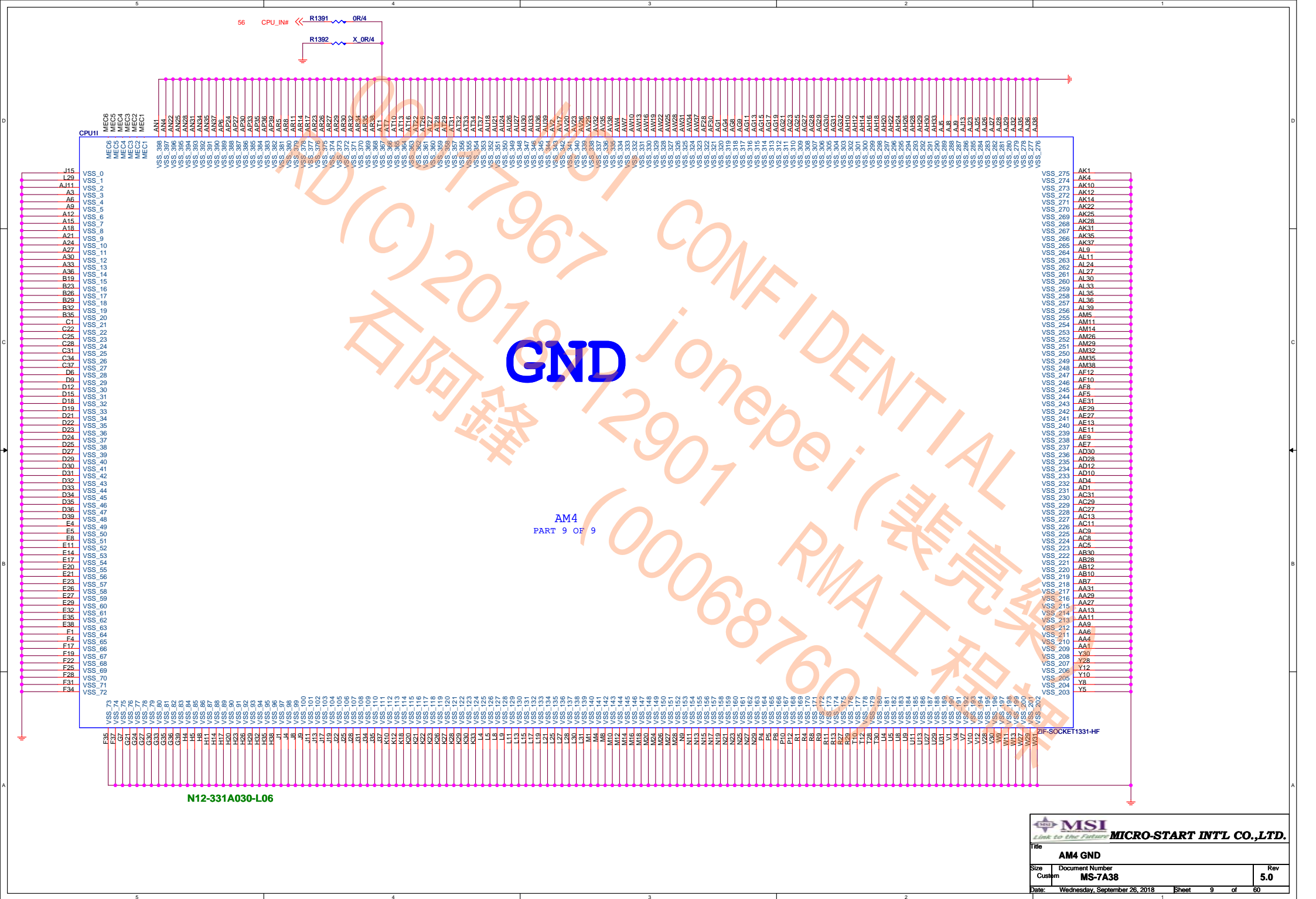


N12-331A030-L06

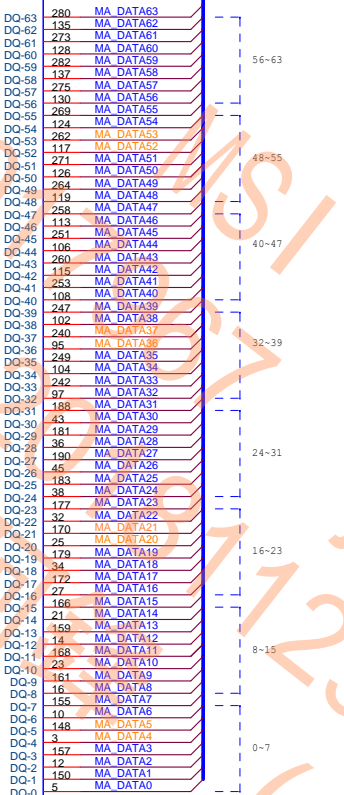
N12-331A030-L06

AM4

ZIF-SOCKET1331-HF



A1 A2 B1 B2

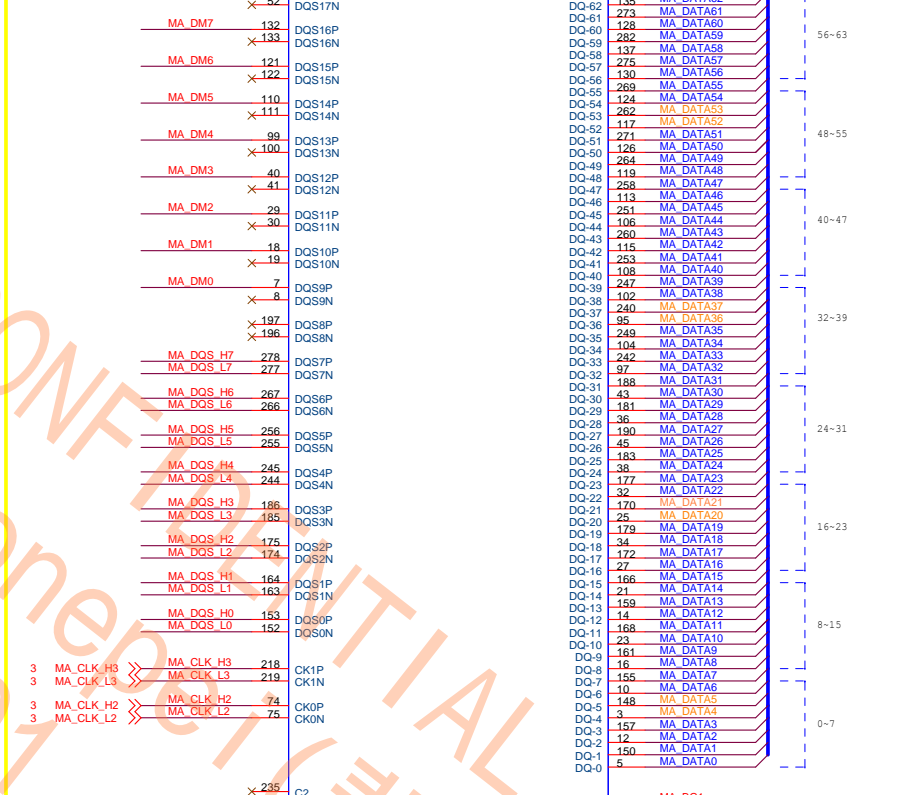


MA_DATA[63:0] 3

MA_ADD[13:0] 3

SMBus 0		
Device	8-bit Address (hex)	
DIMMA0	A0	
DIMMA1	A4	
DIMMB0	A2	
DIMMB1	A6	

DIMM1 (CHANNEL-A) -A0
ADDRESS = 0:0 [SA1:SA0]

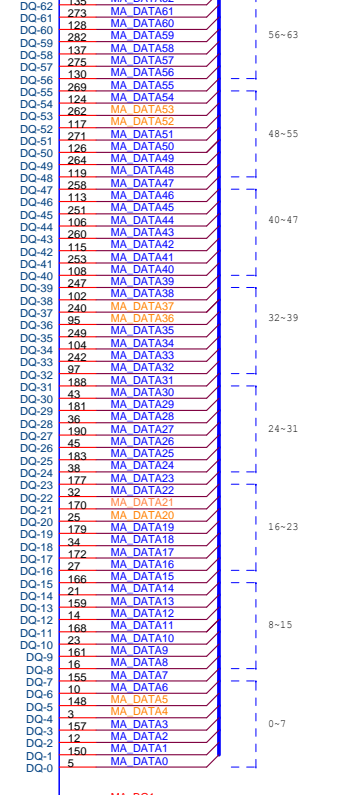


MA_DATA[63:0] 3

MA_ADD[13:0] 3

SMBus 0		
Device	8-bit Address (hex)	
DIMMA0	A0	
DIMMA1	A4	
DIMMB0	A2	
DIMMB1	A6	

DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]



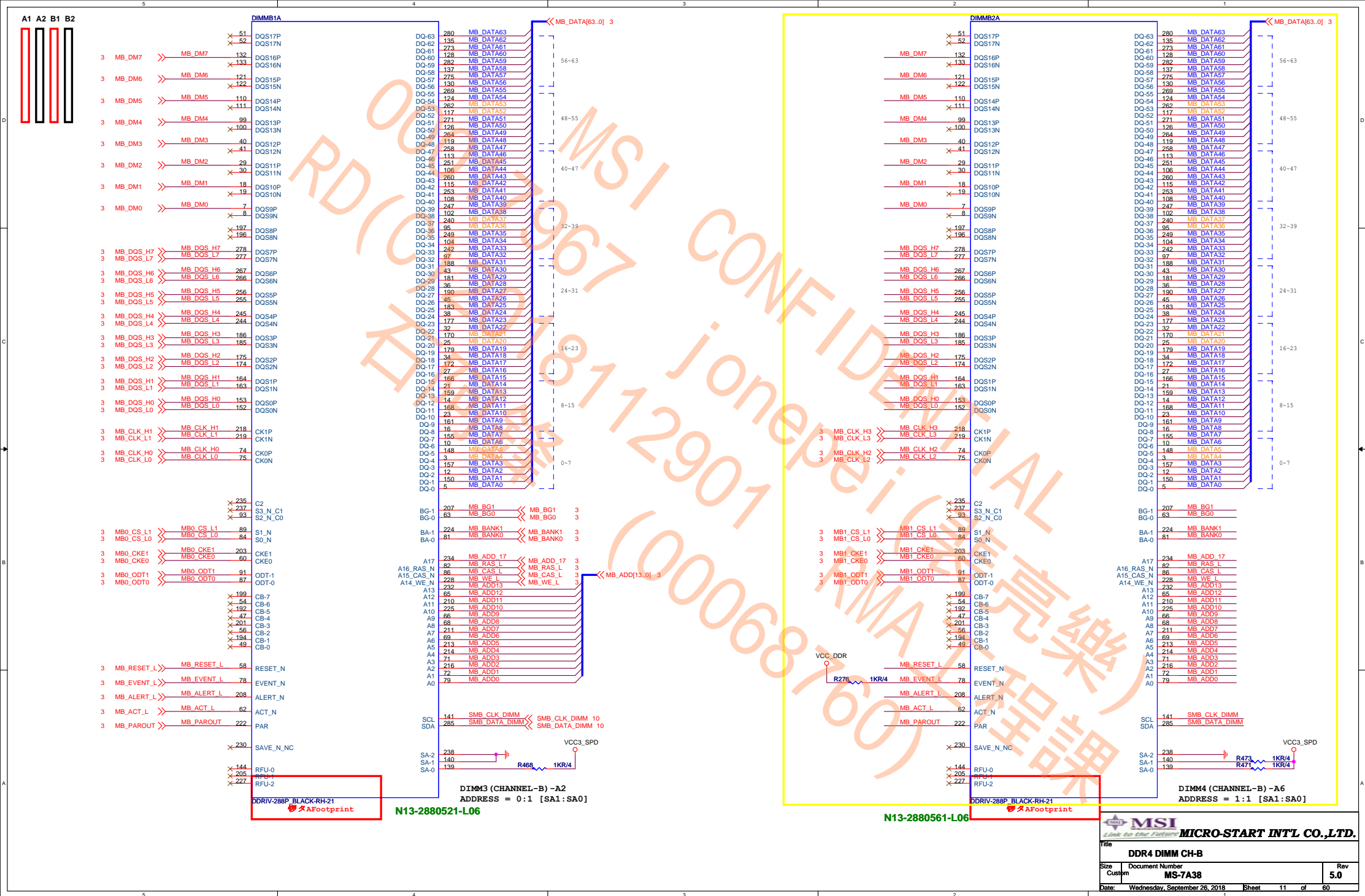
MA_ADD[13:0] 3

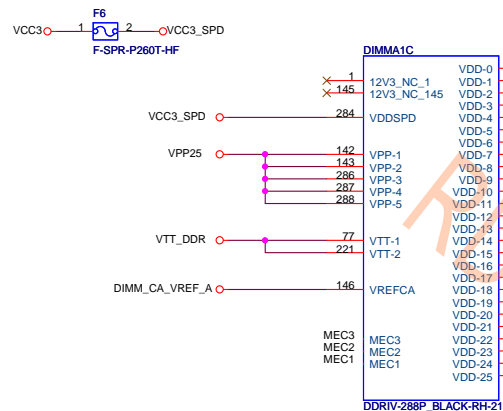
SMBus 0		
Device	8-bit Address (hex)	
DIMMA0	A0	
DIMMA1	A4	
DIMMB0	A2	
DIMMB1	A6	

DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]

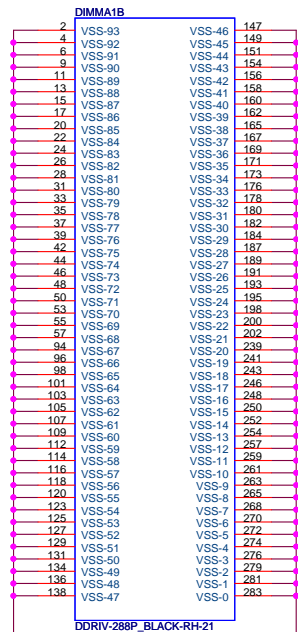
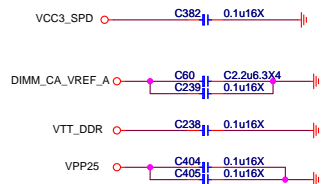


Title		
DDR4 DIMM CH-A		
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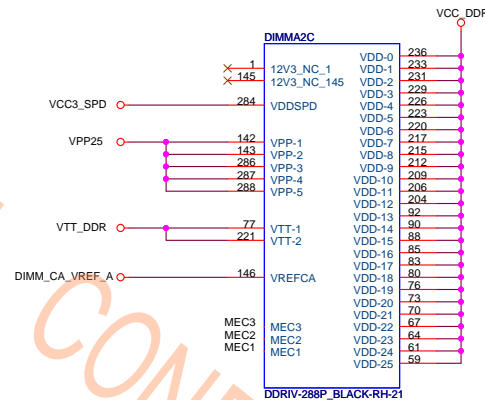




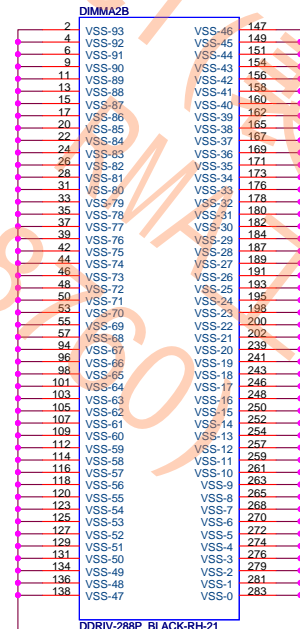
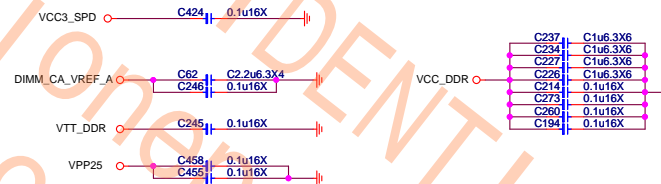
N13-2880521-L06



N13-2880521-L06



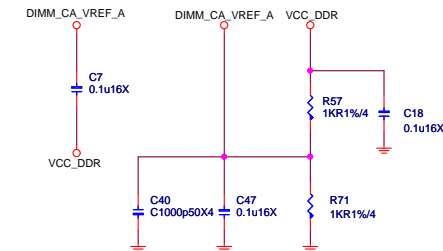
N13-2880561-L06



N13-2880561-L06

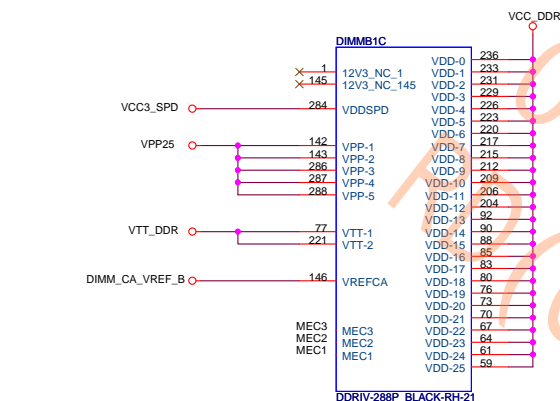
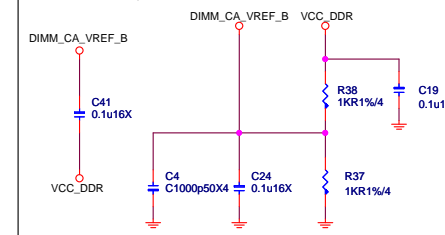
DDR VREF

(place resistors close to DIMMs)

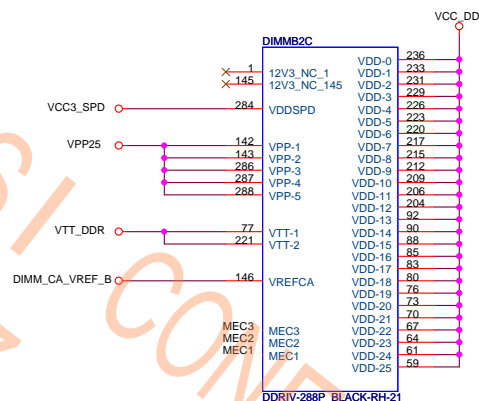
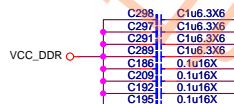
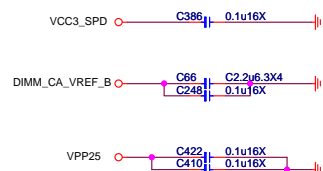


DDR VREF

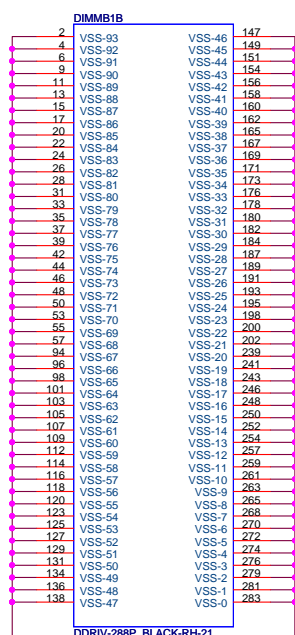
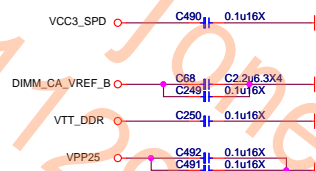
(place resistors close to DIMMs)



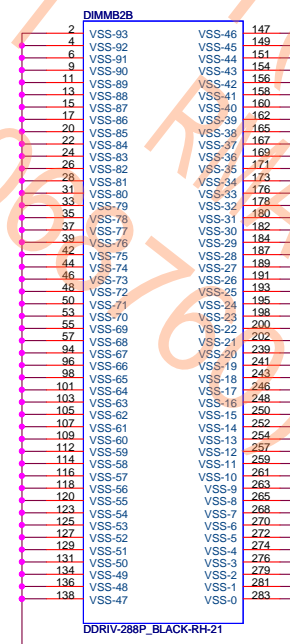
N13-2880521-L06



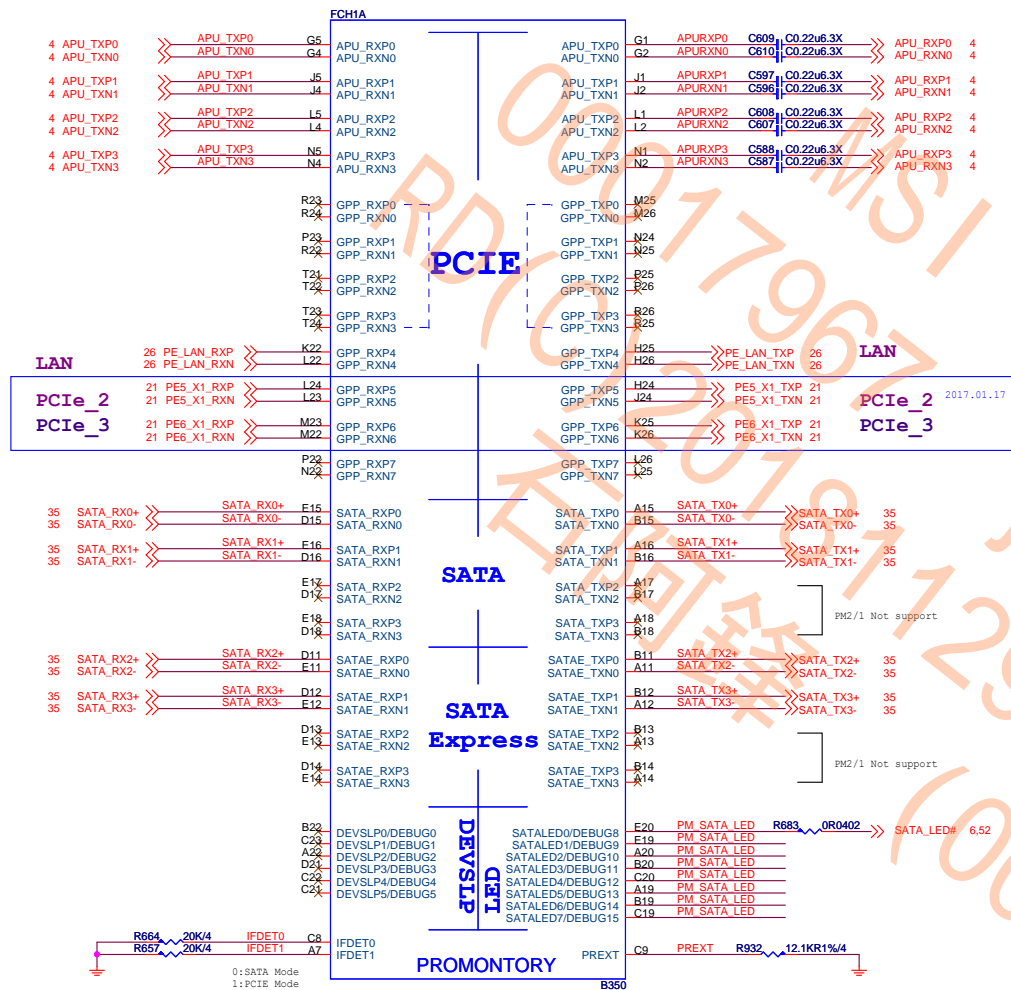
N13-2880561-L06



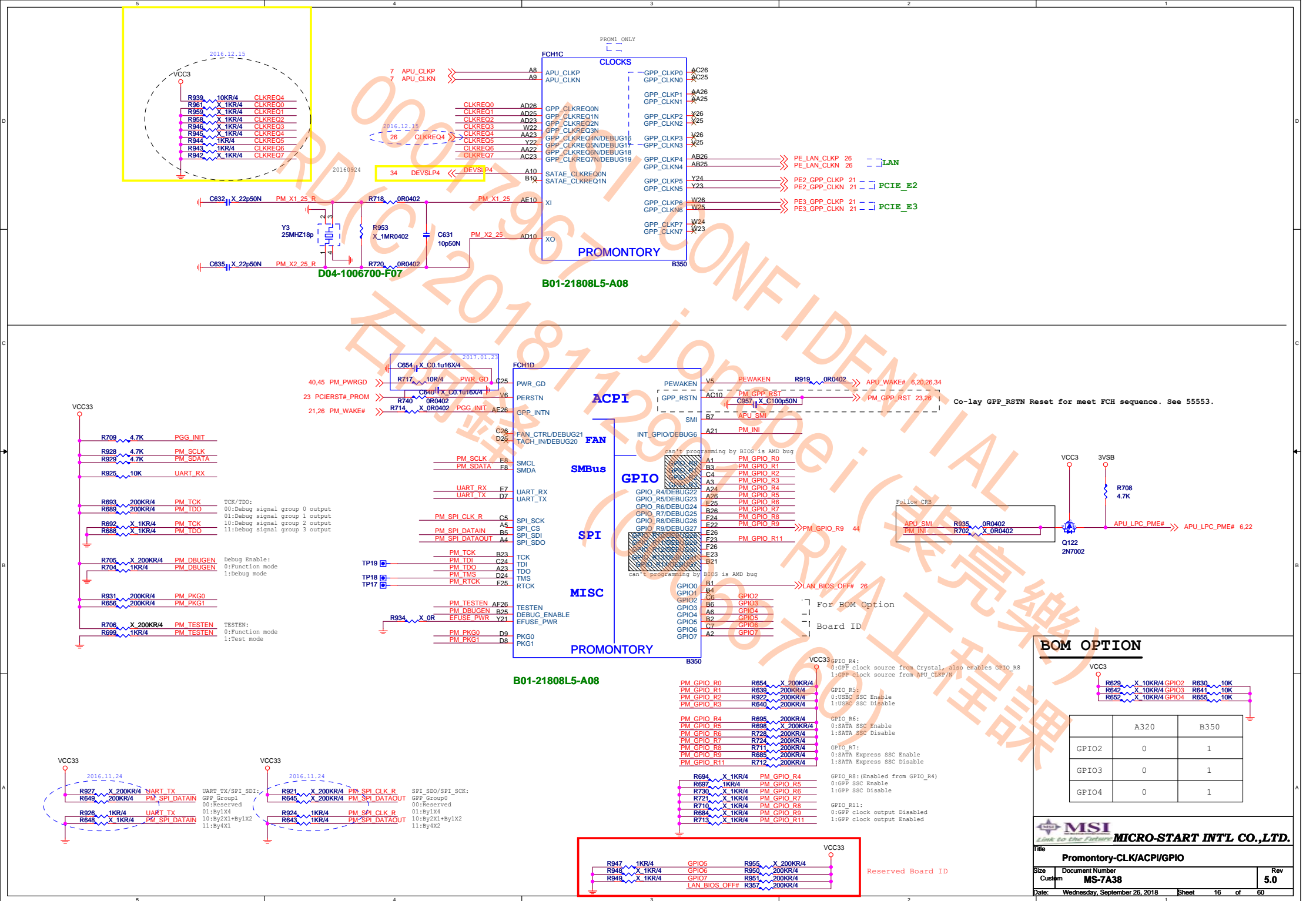
N13-2880521-L06

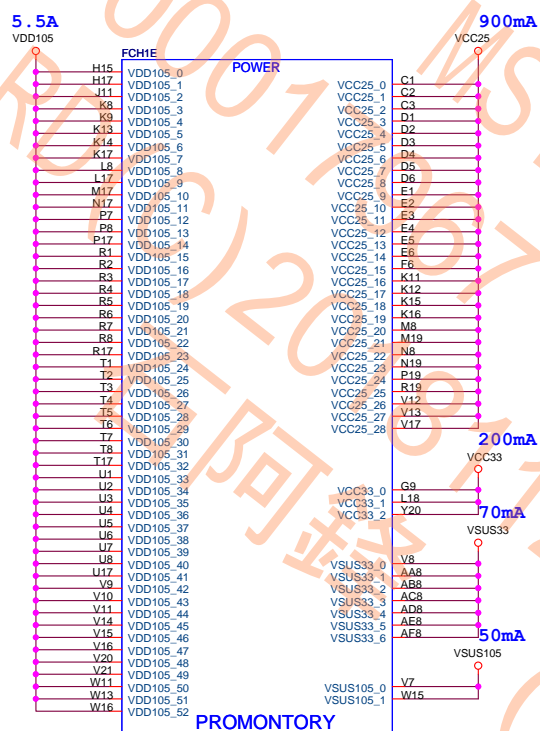
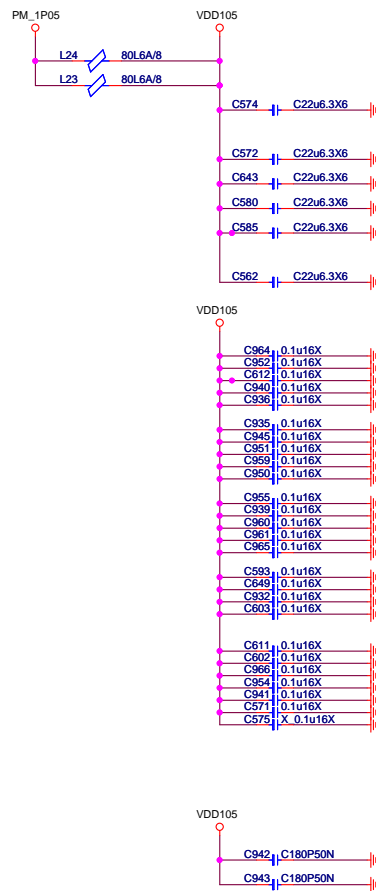


N13-2880561-L06

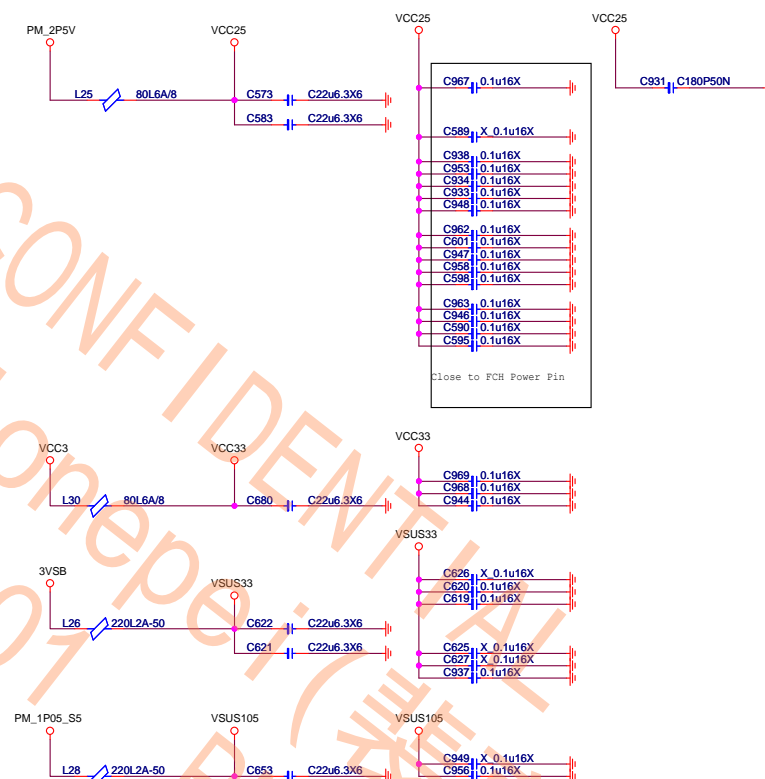


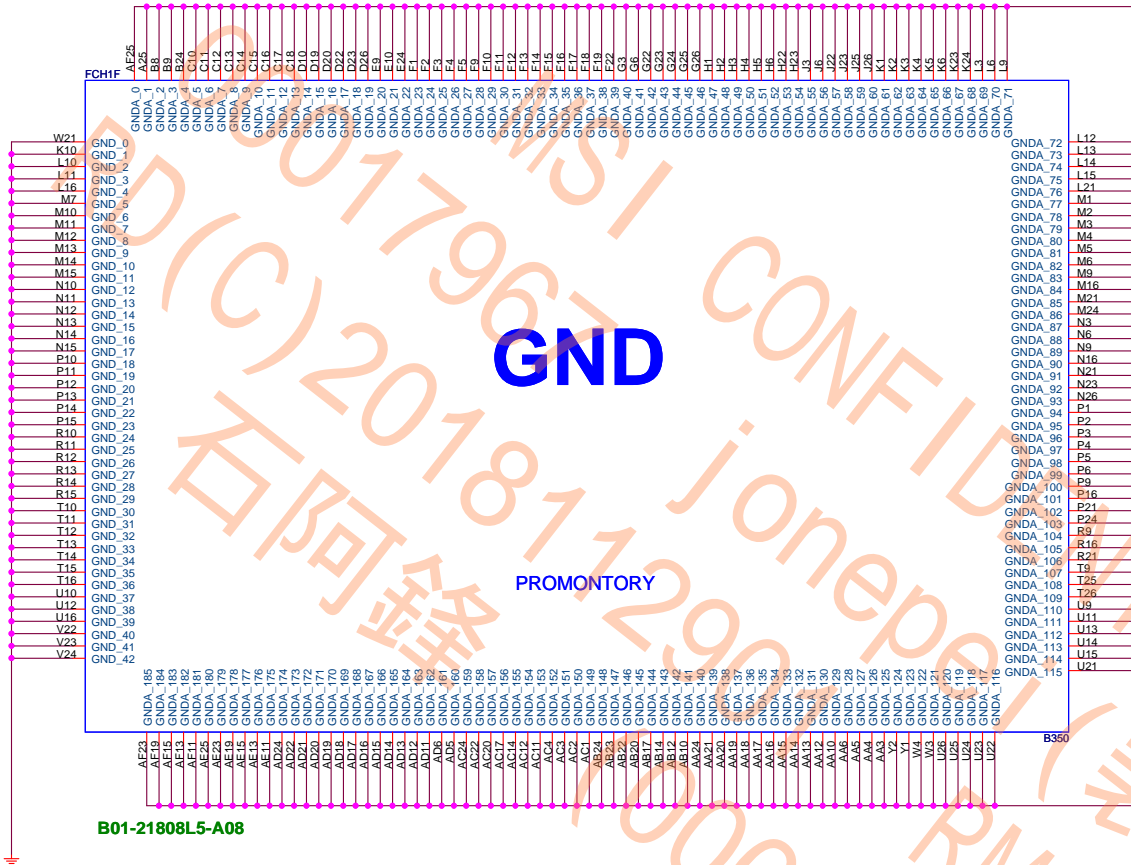
B01-21808L5-A08






B01-21808L5-A08



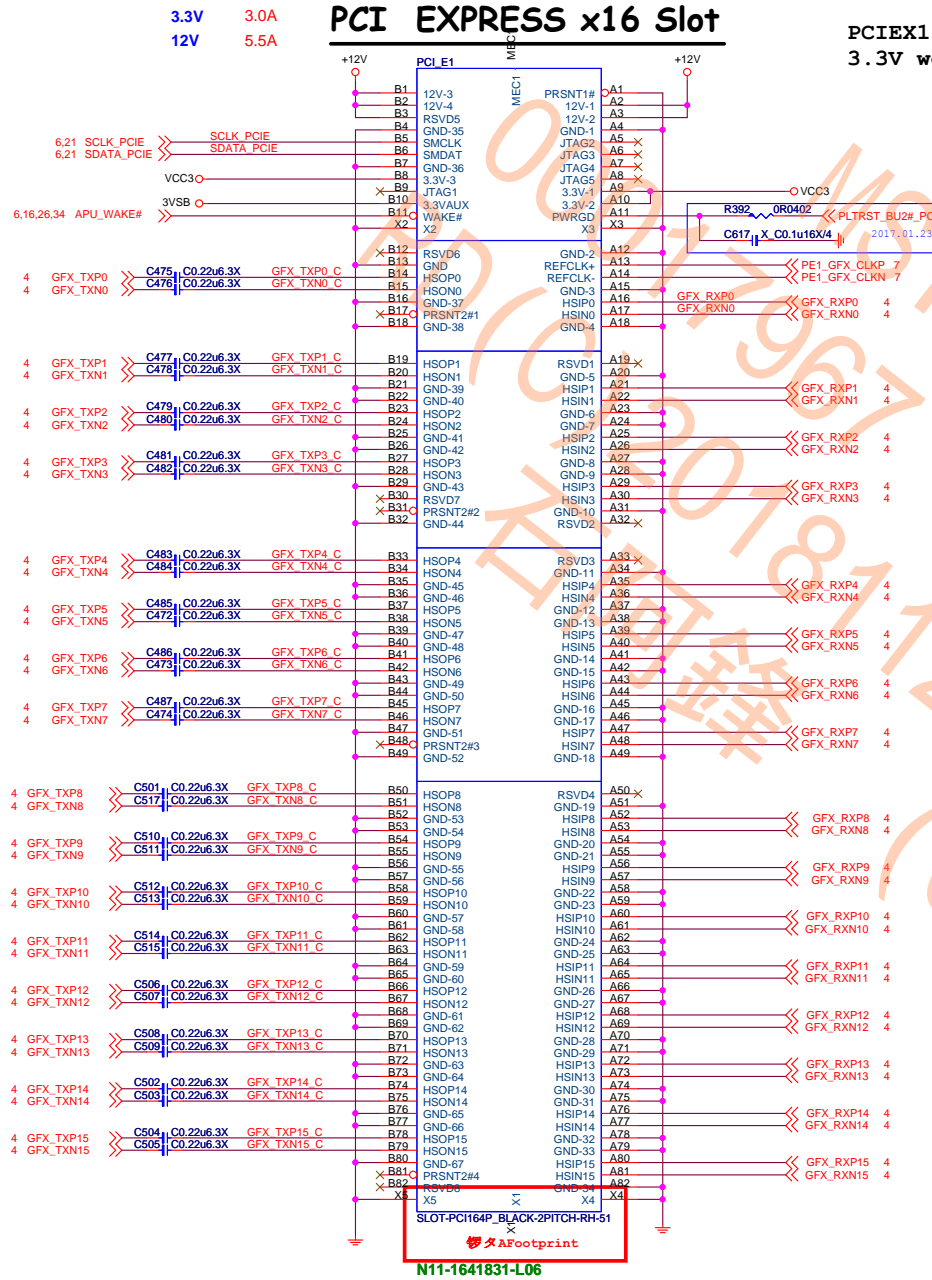


MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2018112901 RMA工程課
石阿鋒 (00068760)

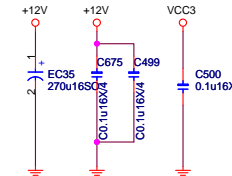
 MICRO-START INTL CO.,LTD.		
Title PCIE CLK		
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PCI EXPRESS x16 Slot

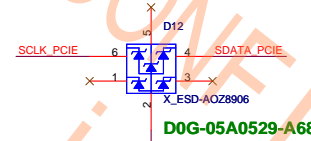
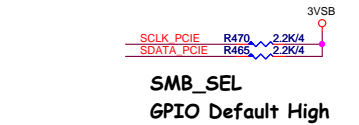
PCIEX1 12V 0.5A
3.3V weak 375mA



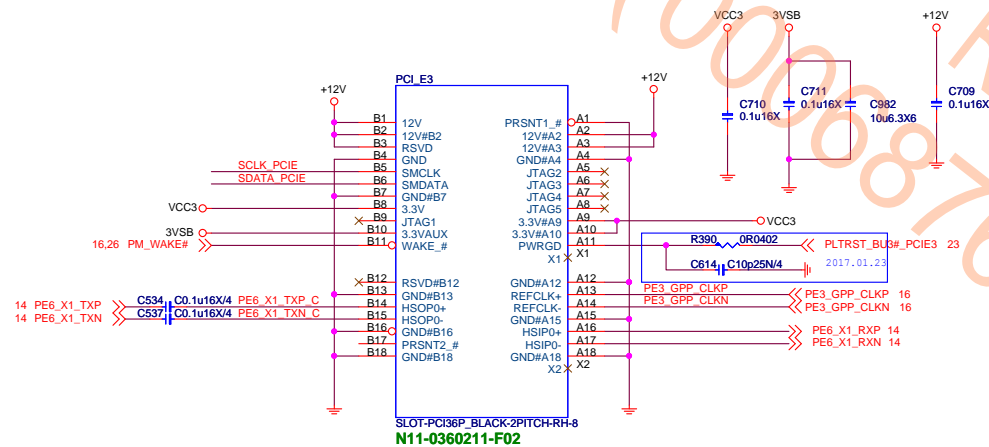
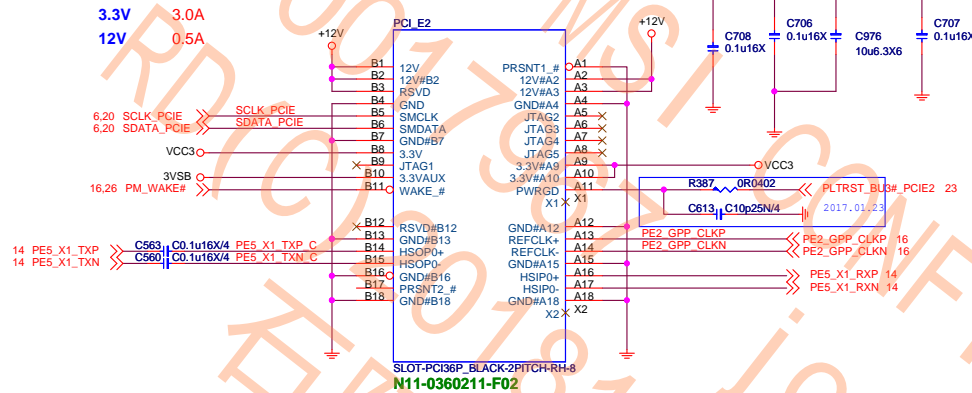
C71-2711891-F70



C71-56106N1-F70



PCIEX1 12V 0.5A
3.3V weak 375mA



PCI Express x1 Slot *2

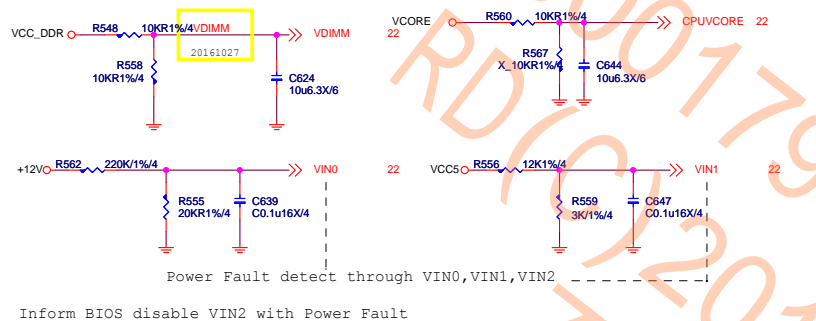
+12V	- 1 A
+VCC3	- 6A
+3V3_S5 (wake)	- 750mA
+3V3_S5 (no wake)	- 40mA

MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

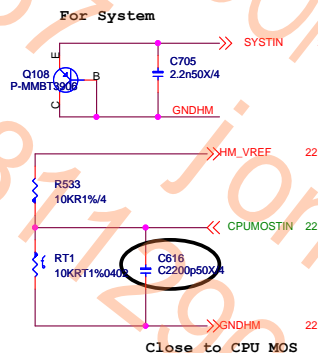
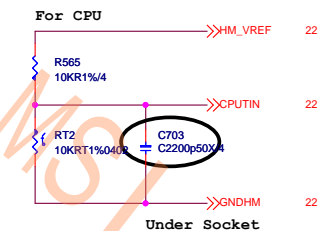
Title PCIE X4(X1*2) SLOT		
Size Custom	Document Number MS-7A38	Rev 5.0
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HW Monitor - Voltage

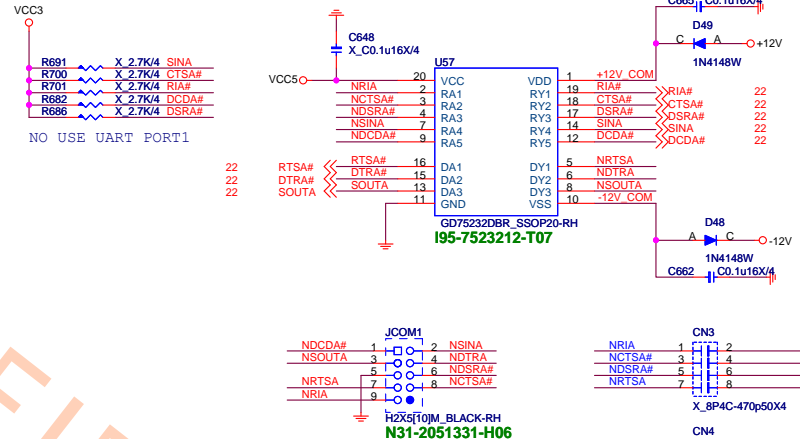
SIO HM Voltage over 2.048V will not detect



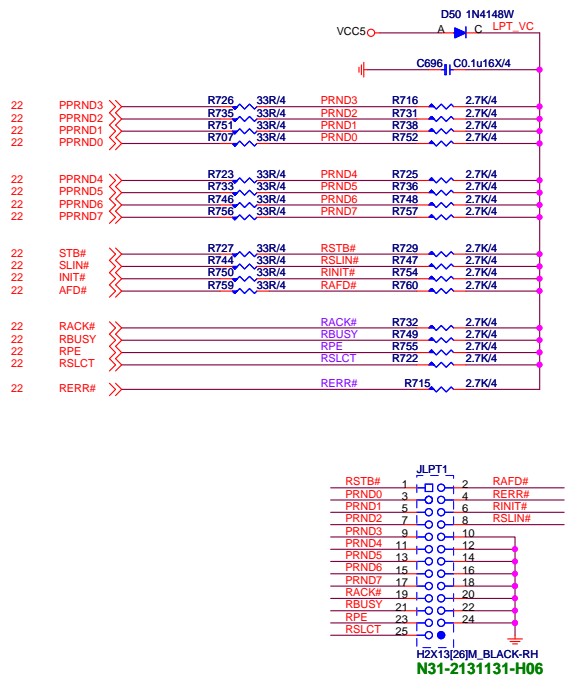
TEMP SENSOR



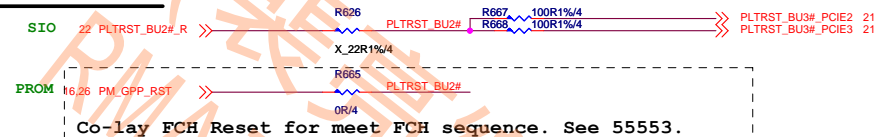
COM PORT



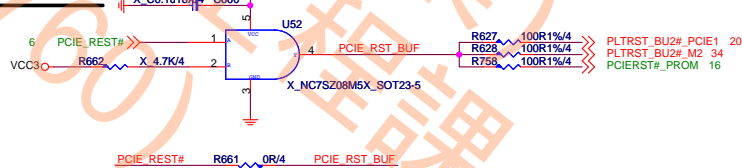
PARALLAL PORT



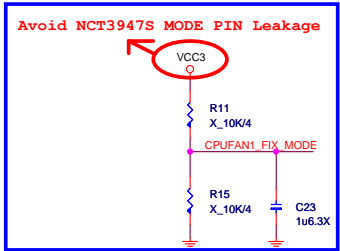
PROM RESET



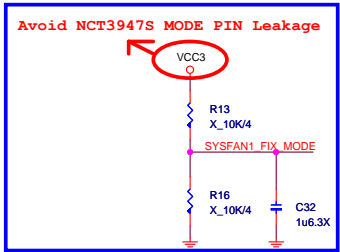
CPU RESET



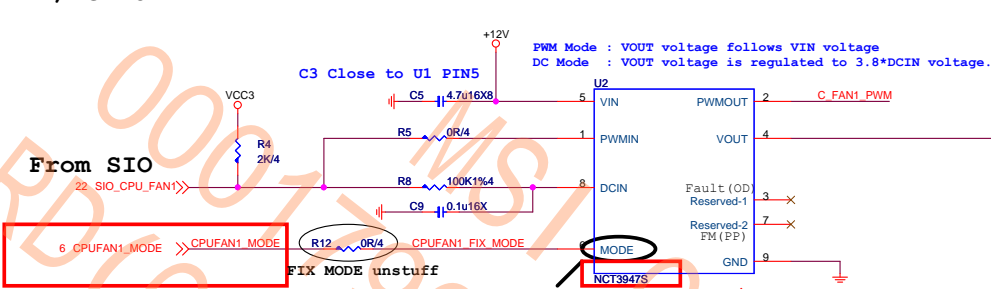
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE
2.GPIO バイオスで PWM/DC MODE



Resever For FIX DC or PWM MODE USE By PM SPEC



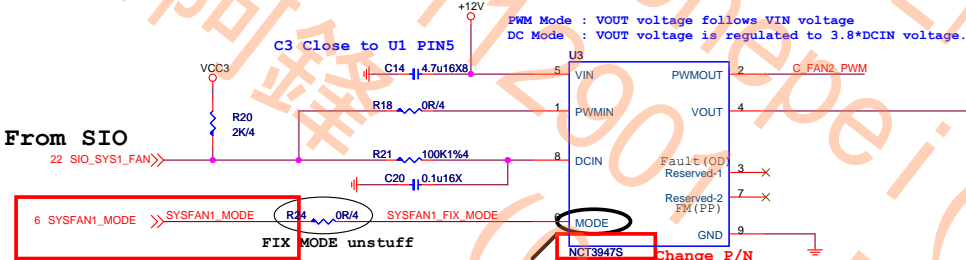
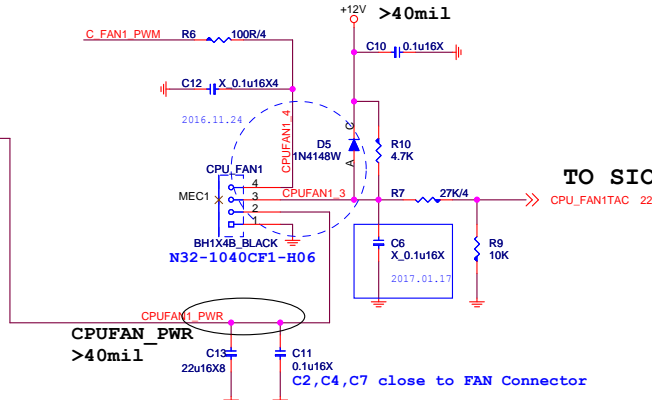
Resever For FIX DC or PWM MODE USE By PM SPEC



GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

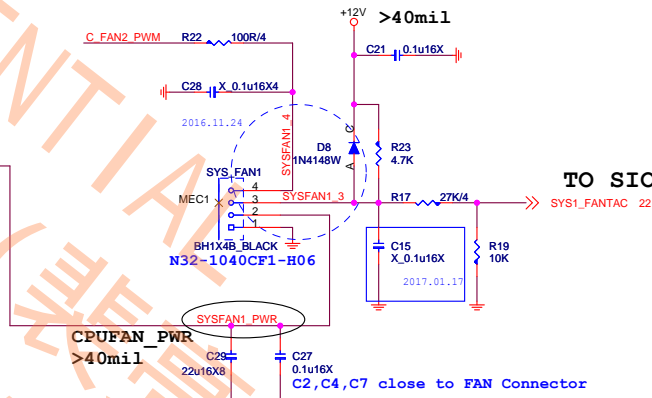
Internall pull up 1.65V

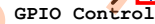
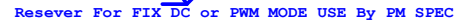


GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

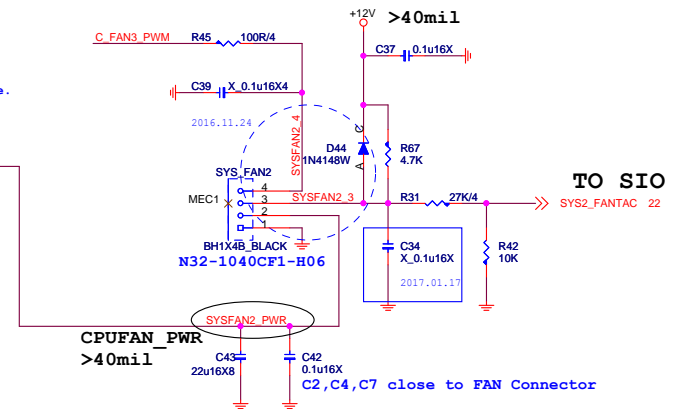
Internall pull up 1.65V





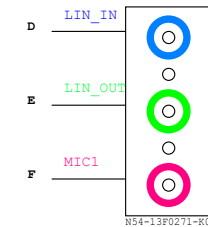
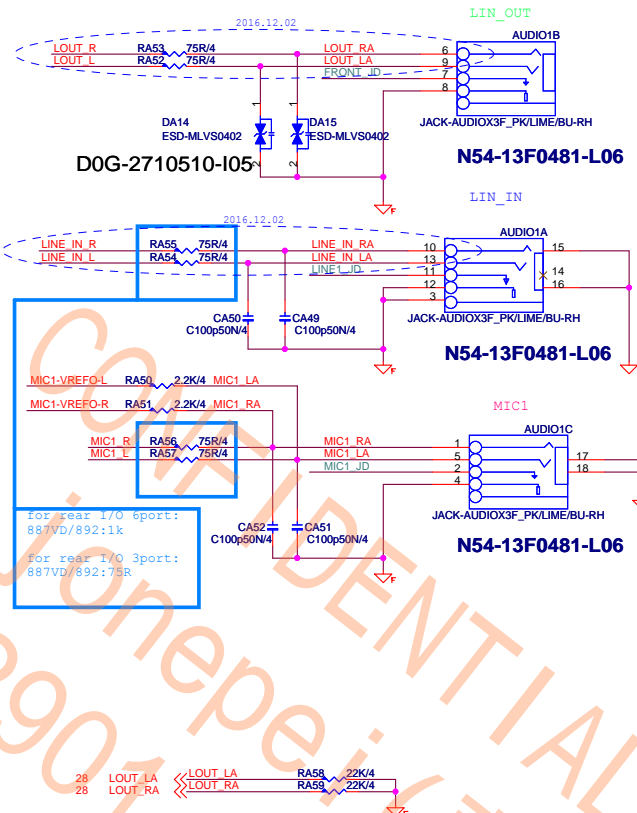
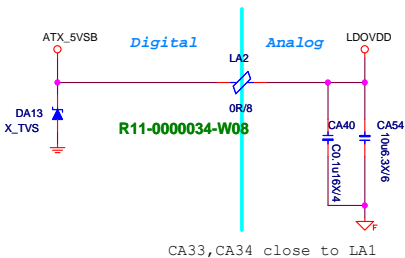
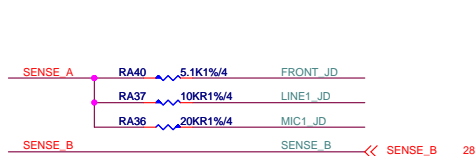
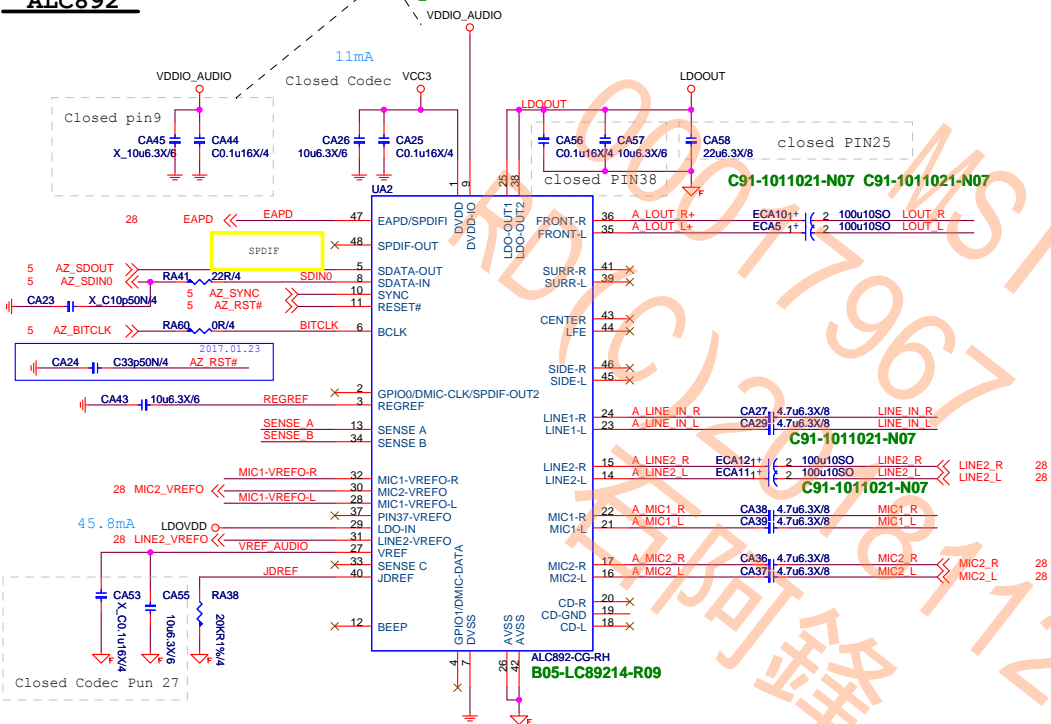
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

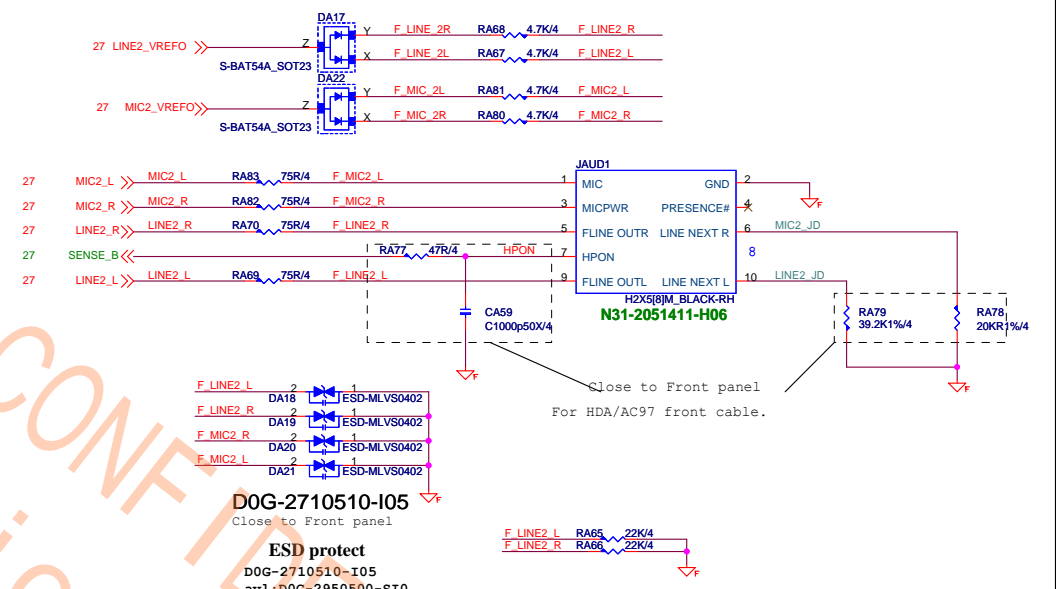
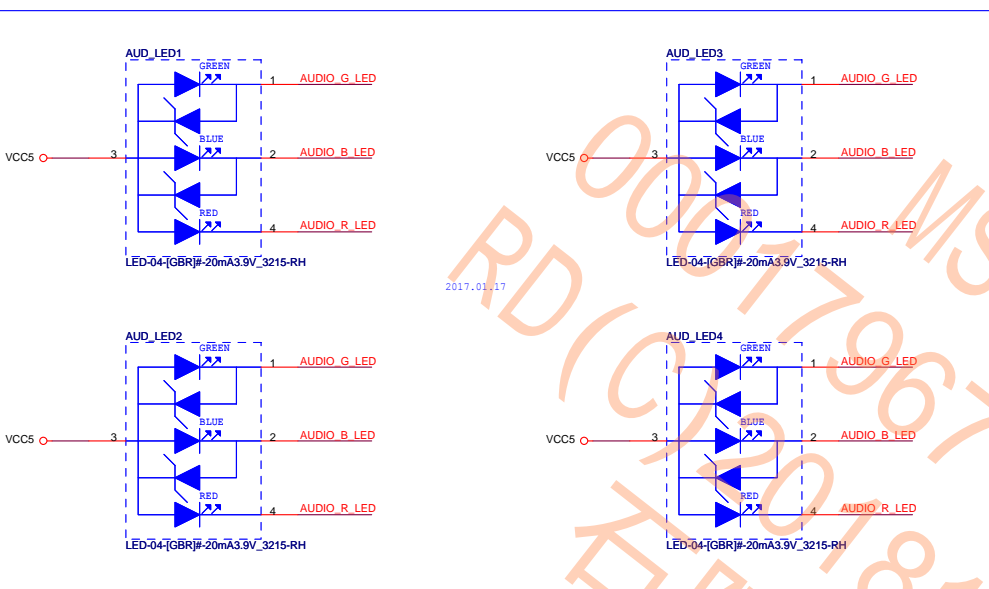
Internall pull up 1.65V



ALC892

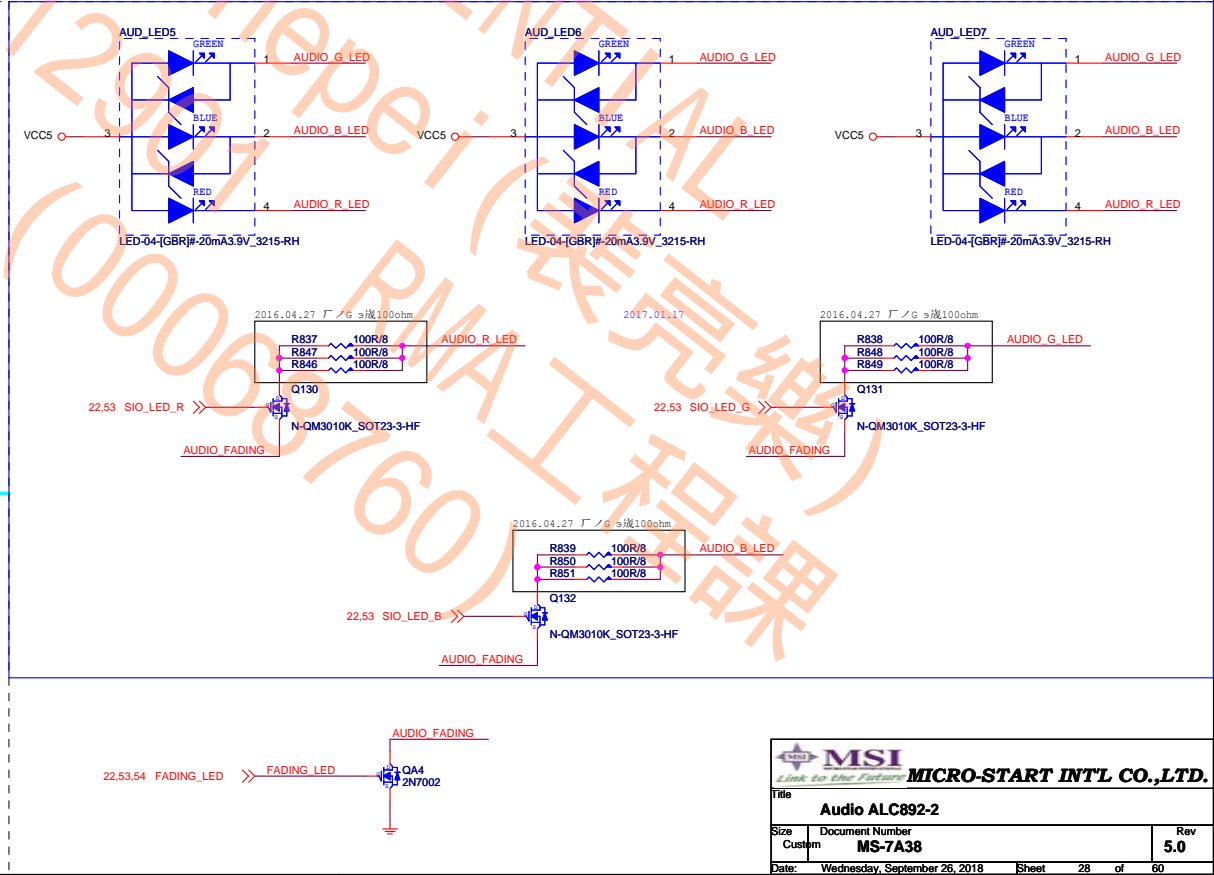
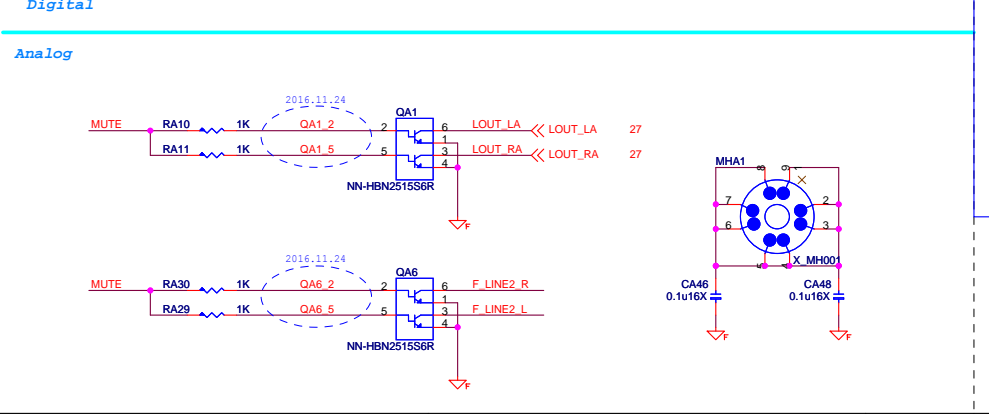
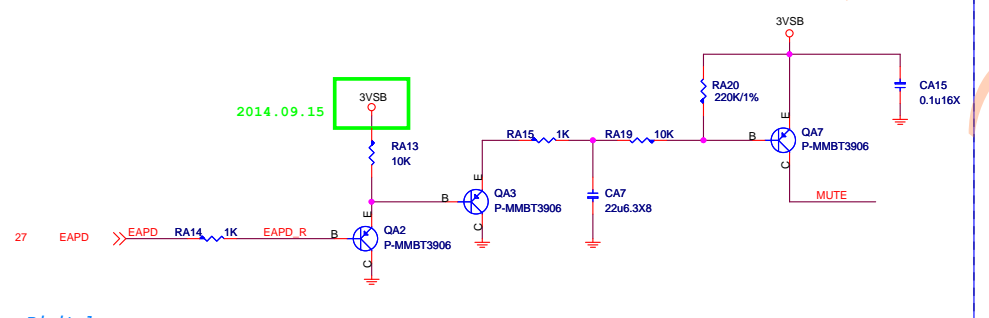
Follow APU power well



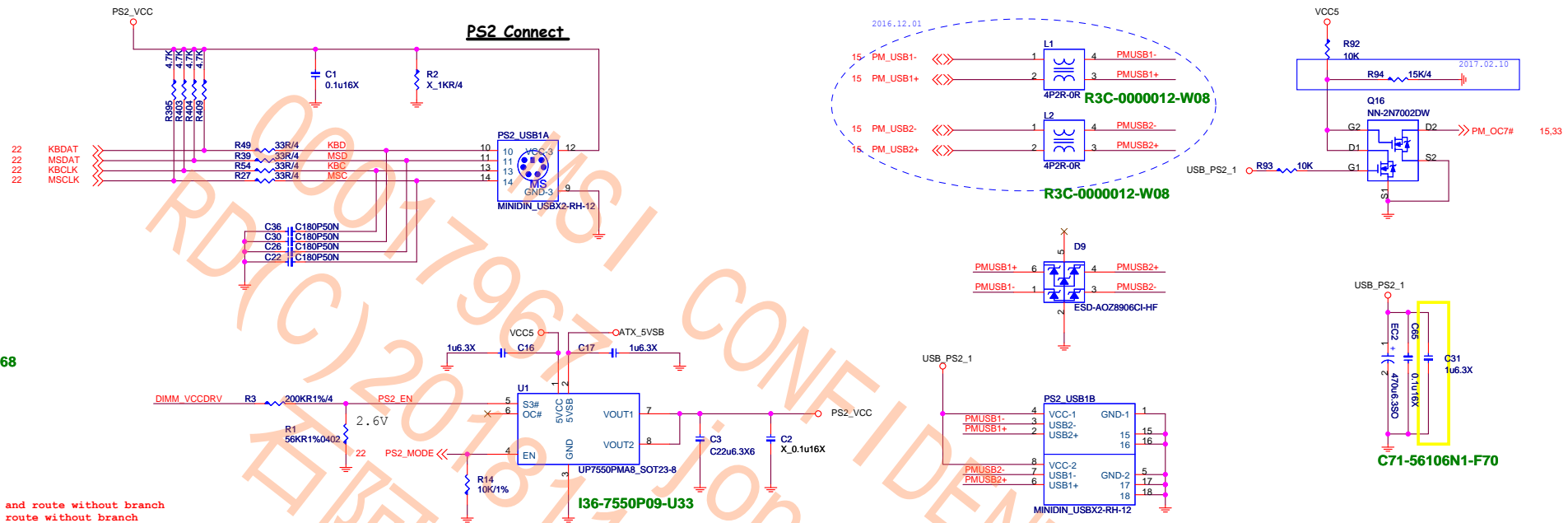


Rear Line OUT De-POP circuit

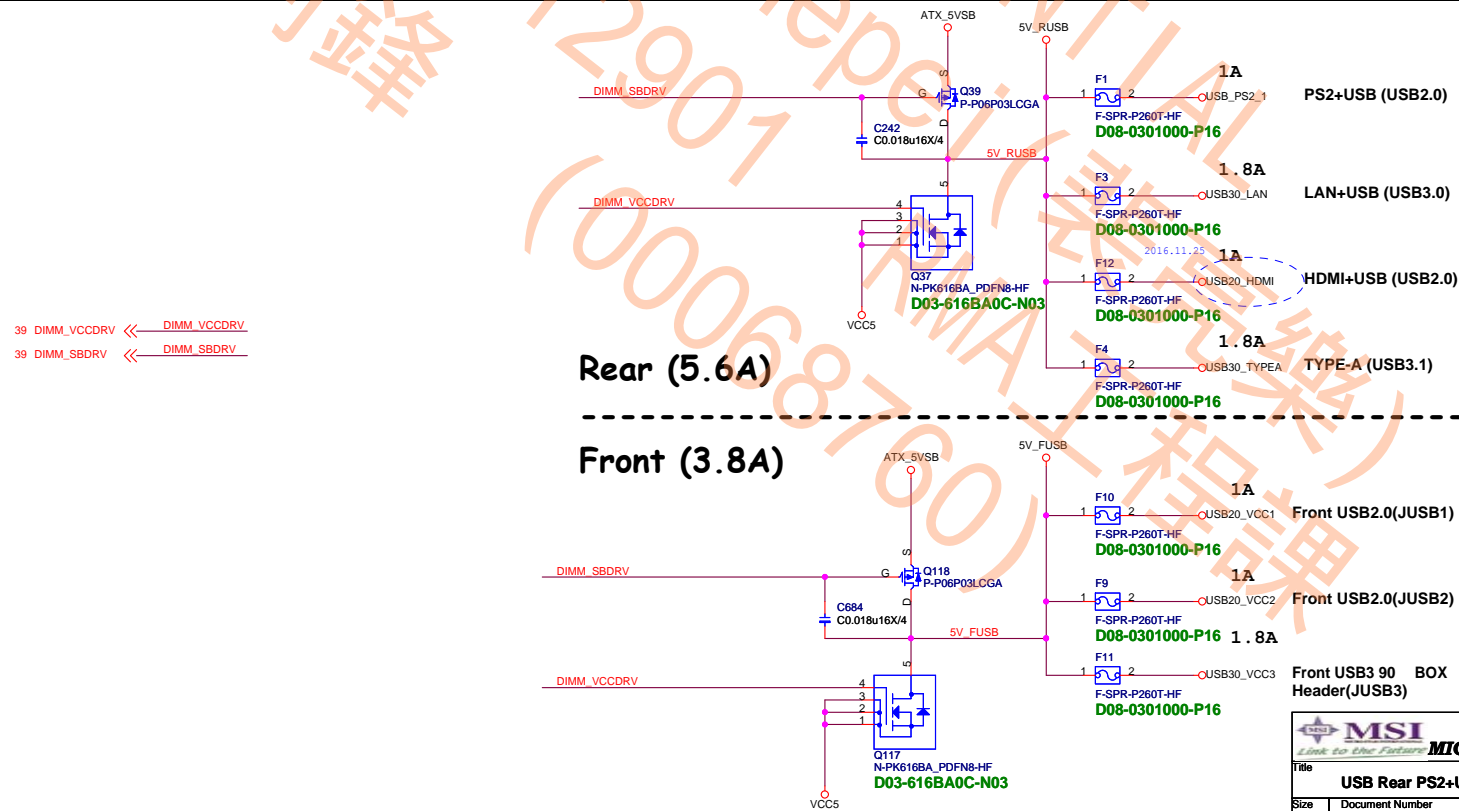
De-pop circuit for Rear Line out & Front Headphone out)



PS2+USB



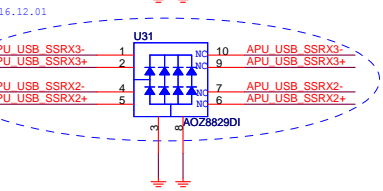
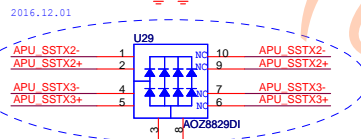
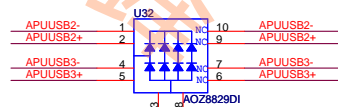
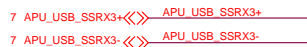
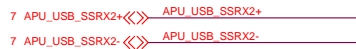
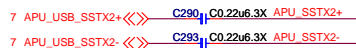
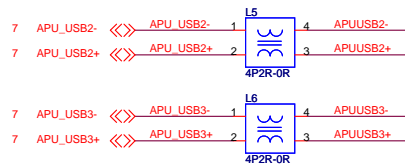
USB Power



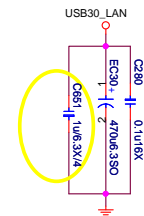
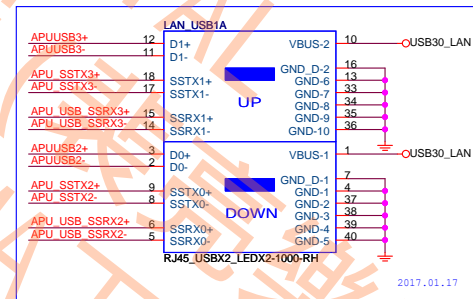
USB3.1 GEN1

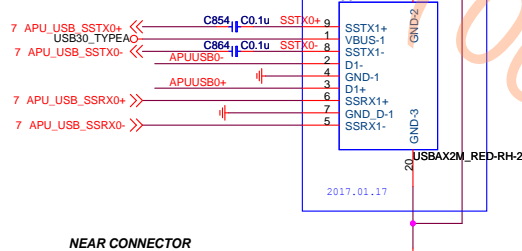
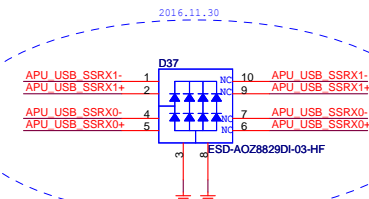
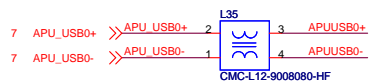
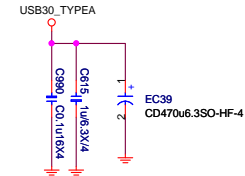
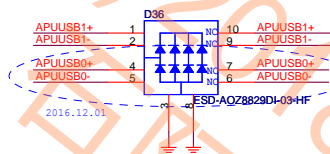
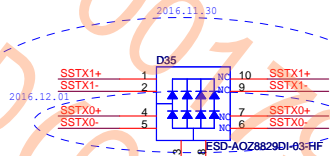
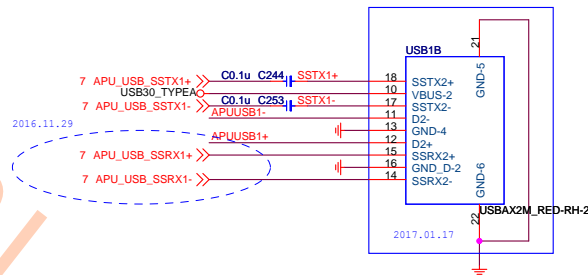
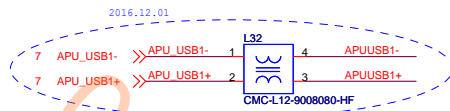
VR Sloution U2 redriver

00017967 MSI CONFIDENTIAL
RD(C)2018112901 jonepei
石阿鋒 (00068760) RMA工程課

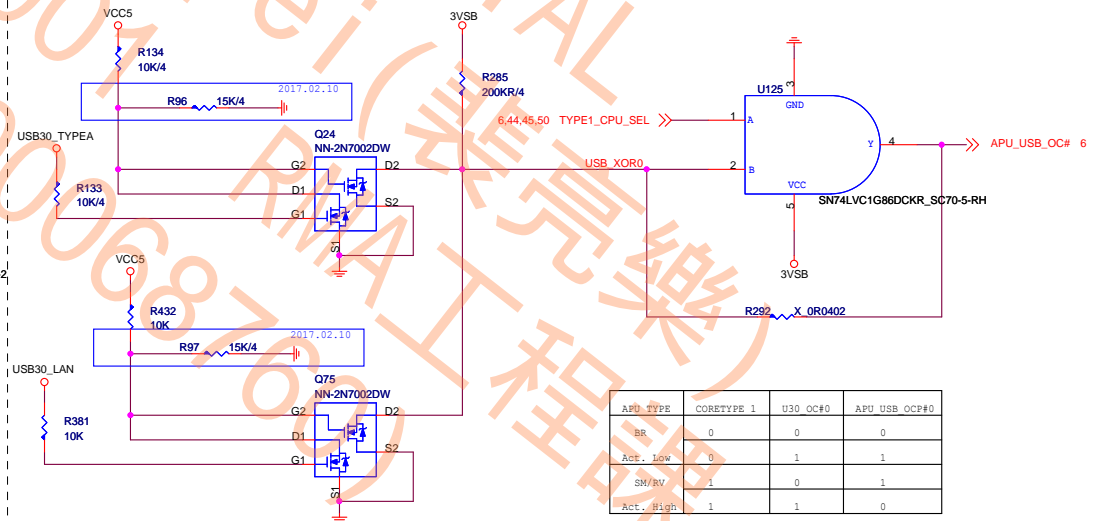


LAN+USB



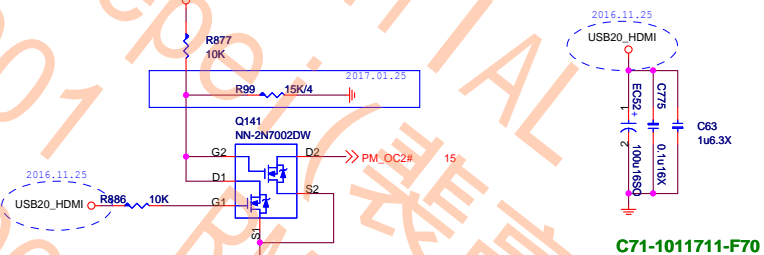
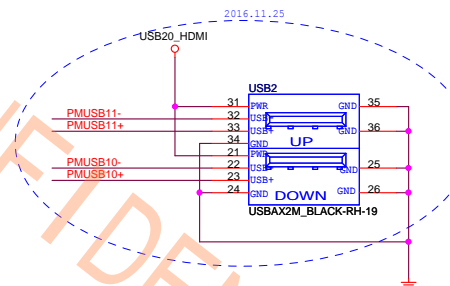
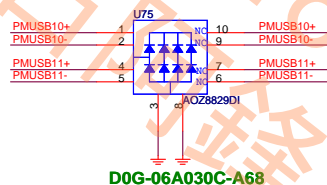
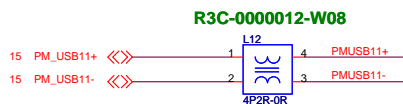
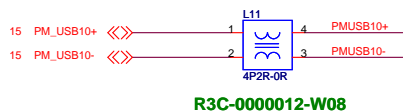


NEAR CONNECTOR

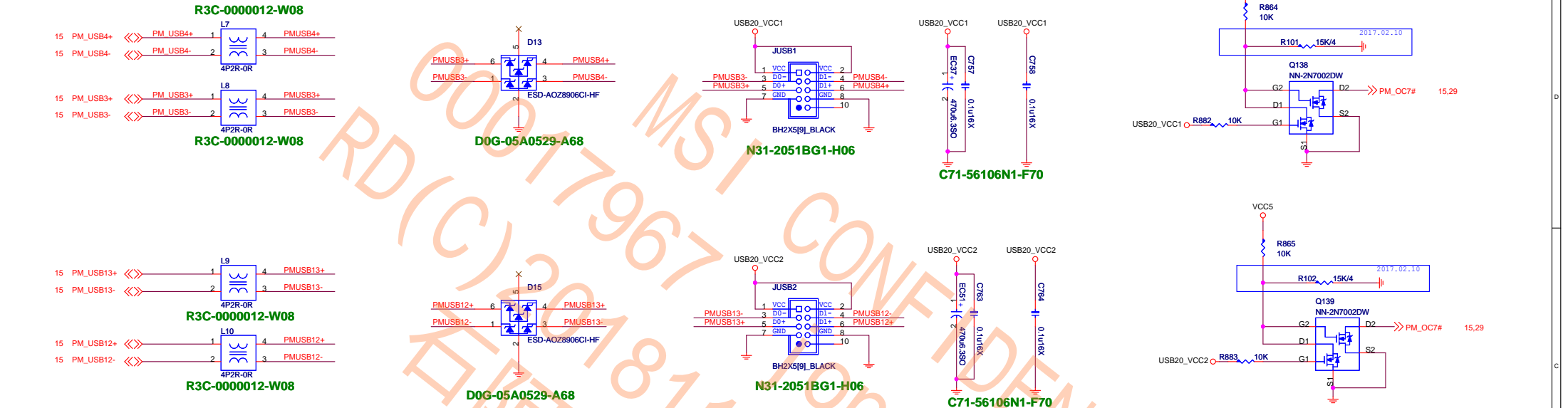


APU_TYPE	CORETYPE 1	U30_OC#0	APU_USB_OC#0
BR	0	0	0
Act. Low	0	1	1
SM/RV	1	0	1
Act. High	1	1	0

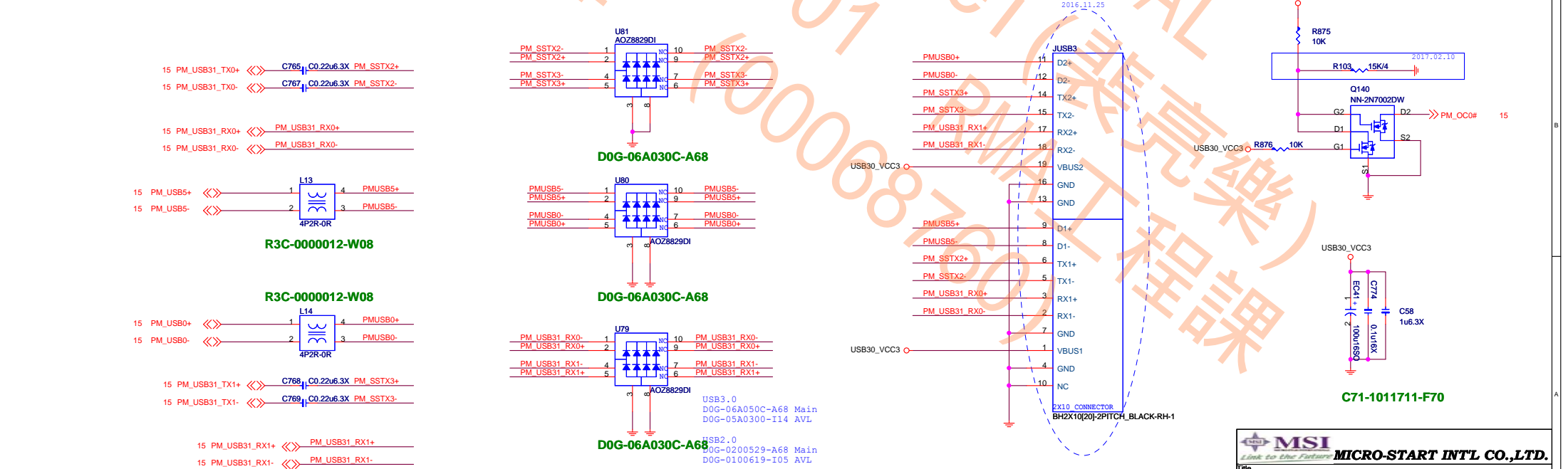
Front USB2.0



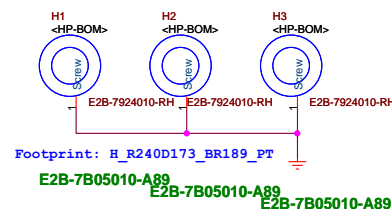
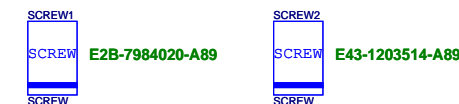
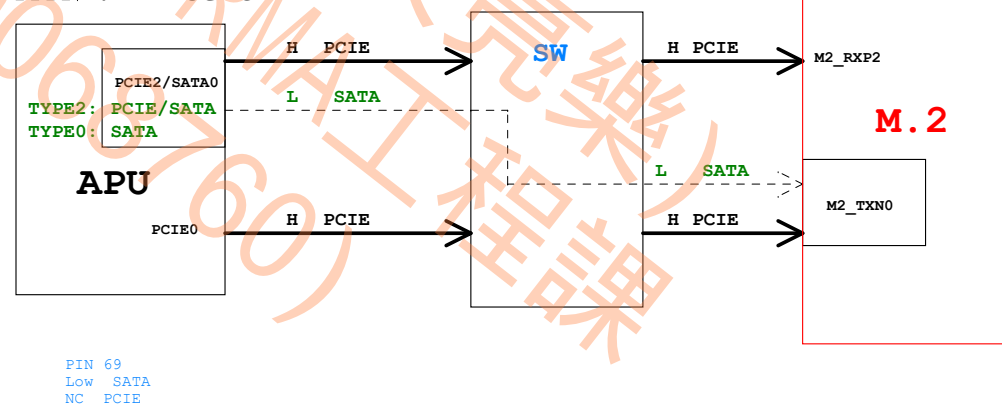
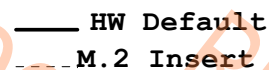
Front USB2.0



Front USB3.1 GEN1

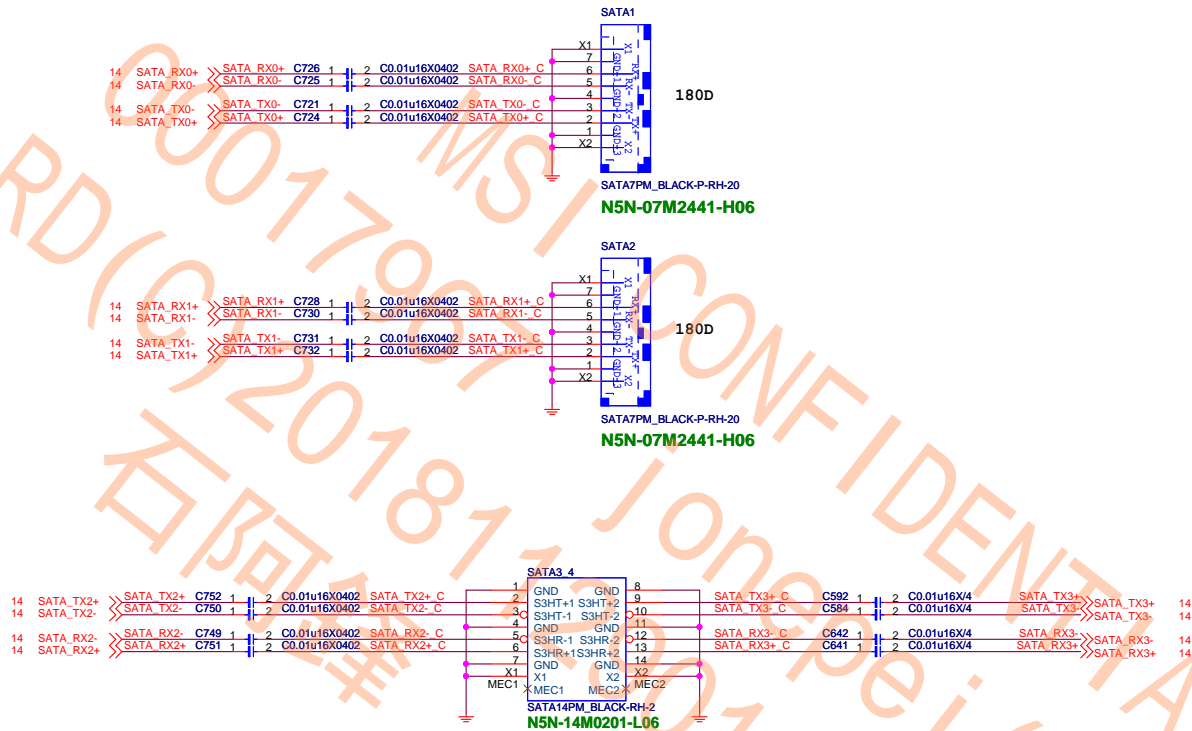


3.3V@2.5A



SW:
H:M.2 PCIE
L:M.2 SATA

SATA Connector



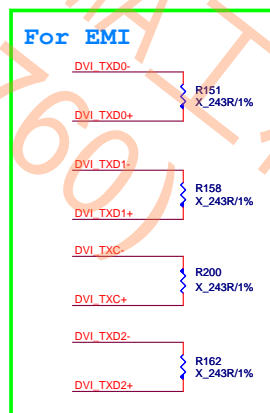
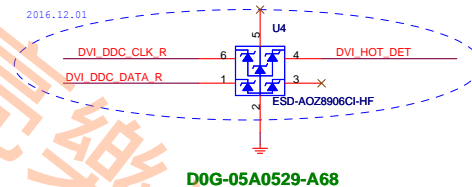
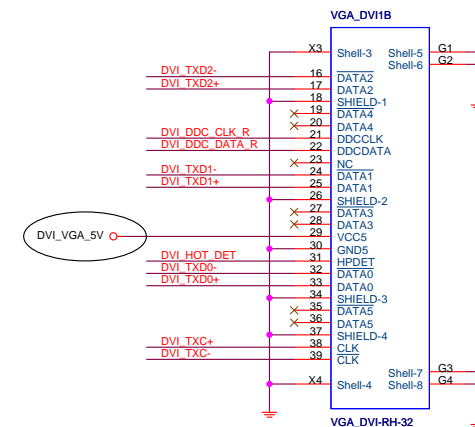
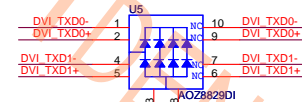
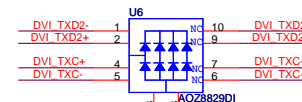
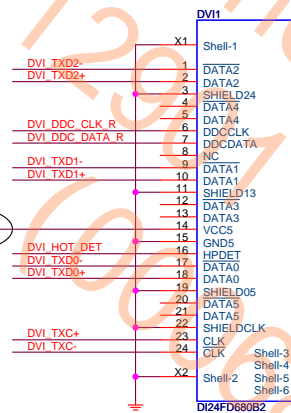
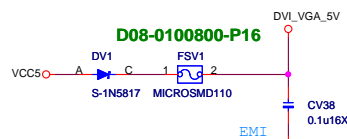
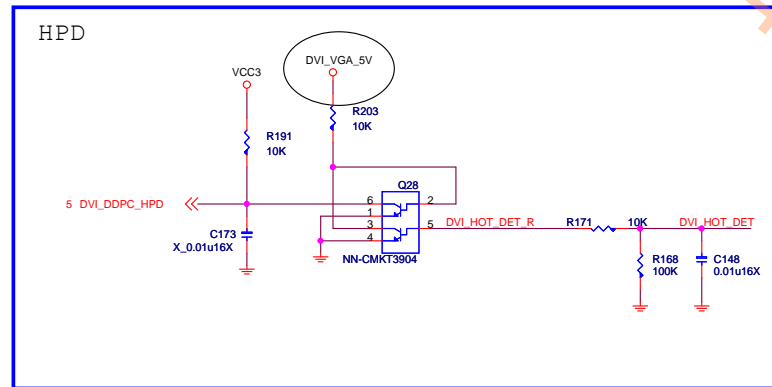
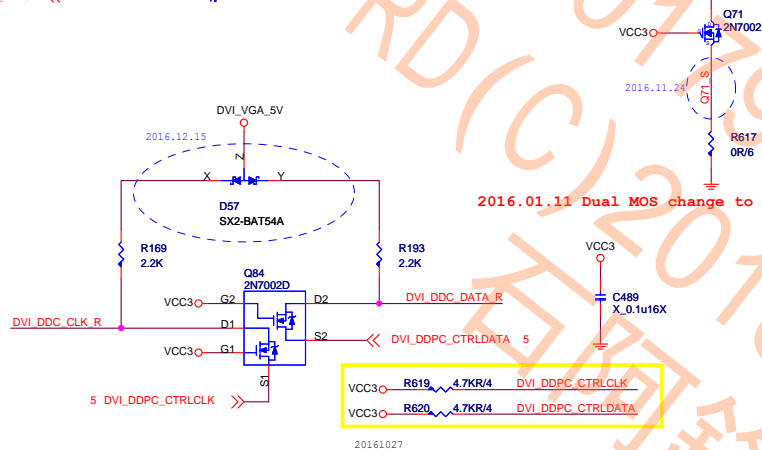
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



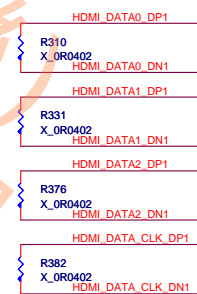
Title DP			
Size Custom	Document Number MS-7A38		Rev 5.0
Date:	Wednesday, September 26, 2018	Sheet 36 of 60	

DVI level shifter

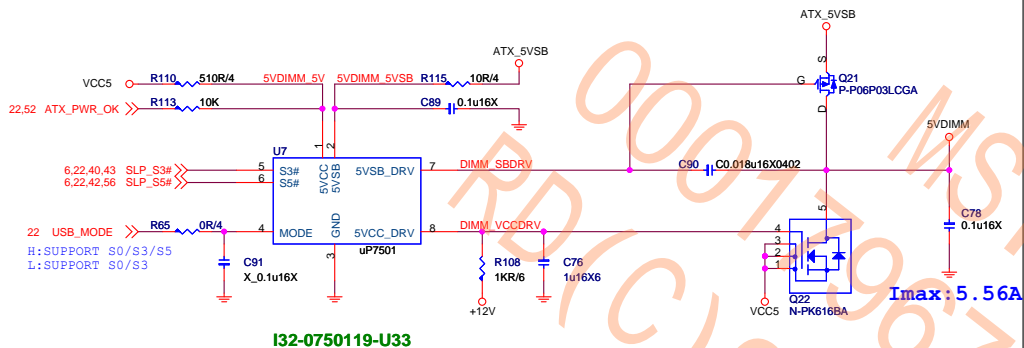
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



For HDMI 1.4



5VDIMM FOR DDR



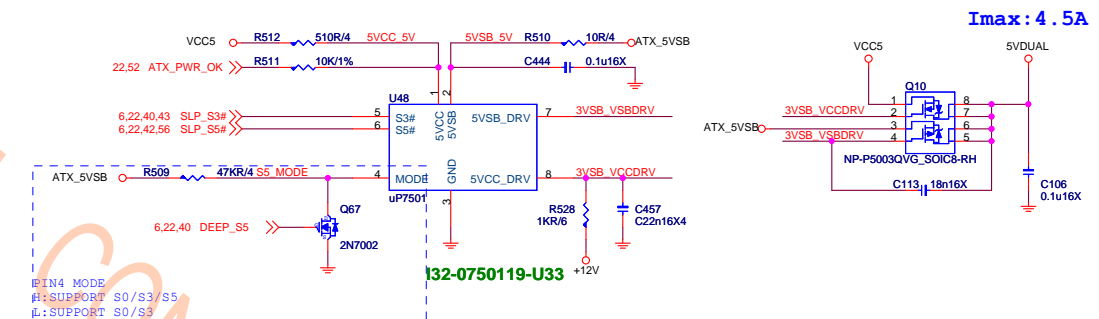
I32-0750119-U33

```

29 DIMM_VCCDRV <<= DIMM_VCCDRV
29 DIMM_SBDREV <<= DIMM_SBDREV

```

5VDUAL For 3VSB CPU 1.8V VDDP

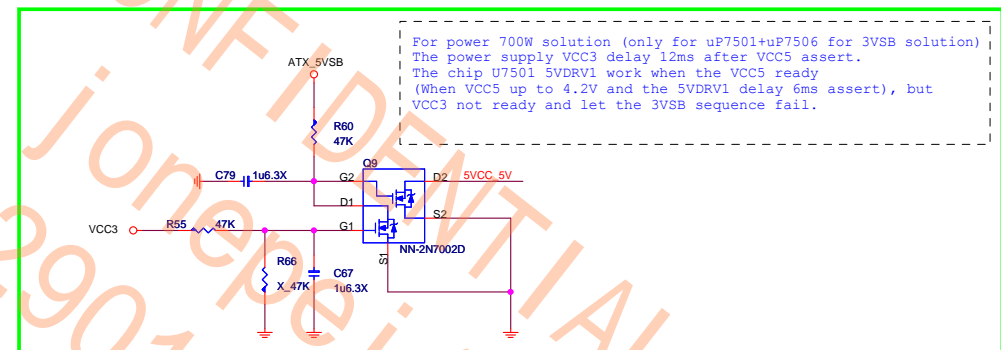


Imax: 4.5A

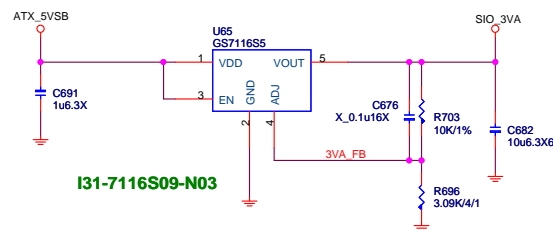
```

r power 700W solution (only for uP7501+uP7506 for 3VSB solution)
e power supply VCC3 delay 12ms after VCC5 assert.
e chip U7501 5VDRV1 work when the VCC5 ready
hen VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
CC3 not ready and let the 3VSB sequence fail.

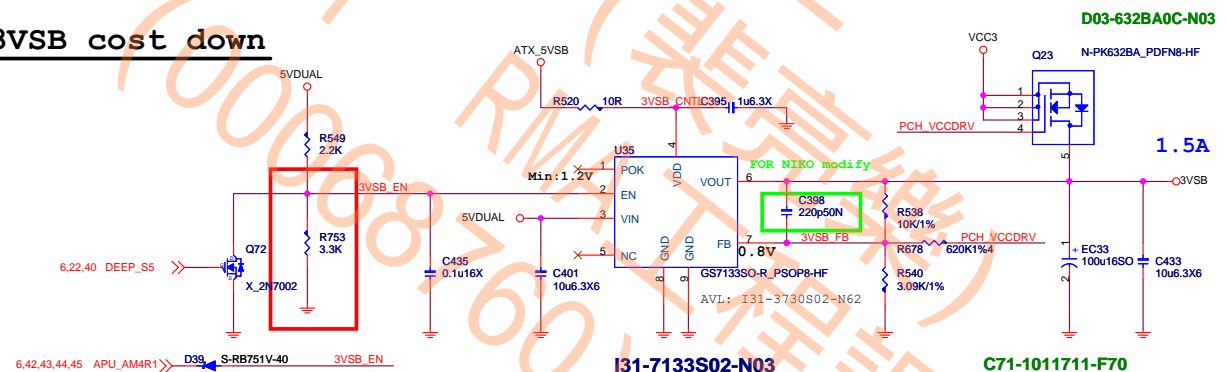
```



3VSB cost down



I31-7116S09-N03

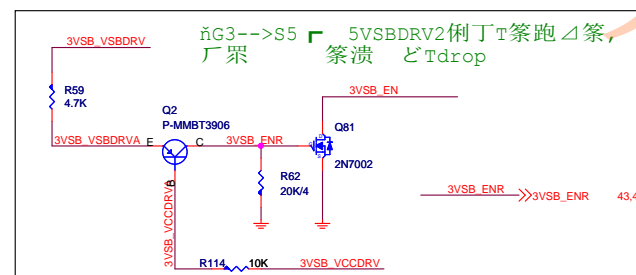


D03-632BA0C-N03

1.5A

I31-7133S02-N03

C71-1011711-F70



ňG3-->S5 𐀓 5VSBDRV2𐀔𐀕𐀖𐀗𐀘𐀙𐀚𐀛𐀜𐀝𐀞𐀟𐀠𐀡𐀢𐀣𐀤𐀥𐀦𐀧𐀨𐀩𐀪𐀫𐀬𐀭𐀮𐀯𐀰𐀱𐀲𐀳𐀴𐀵𐀶𐀷𐀸𐀹𐀺𐀻𐀼𐀽𐀾𐀿𐁀𐁁𐁂𐁃𐁄𐁅𐁆𐁇𐁈𐁉𐁊𐁋𐁌𐁍𐁎𐁏𐁐𐁑𐁒𐁓𐁔𐁕𐁖𐁗𐁘𐁙𐁚𐁛𐁜𐁝𐁞𐁟𐁠𐁡𐁢𐁣𐁤𐁥𐁦𐁧𐁨𐁩𐁪𐁫𐁬𐁭𐁮𐁯𐁰𐁱𐁲𐁳𐁴𐁵𐁶𐁷𐁸𐁹𐁺𐁻𐁼𐁽𐁾𐁿𐂀𐂁𐂂𐂃𐂄𐂅𐂆𐂇𐂈𐂉𐂊𐂋𐂌𐂍𐂎𐂏𐂐𐂑𐂒𐂓𐂔𐂕𐂖𐂗𐂘𐂙𐂚𐂛𐂜𐂝𐂞𐂟𐂠𐂡𐂢𐂣𐂤𐂥𐂦𐂧𐂨𐂩𐂪𐂫𐂬𐂭𐂮𐂯𐂰𐂱𐂲𐂳𐂴𐂵𐂶𐂷𐂸𐂹𐂺𐂻𐂼𐂽𐂾𐂿𐃀𐃁𐃂𐃃𐃄𐃅𐃆𐃇𐃈𐃉𐃊𐃋𐃌𐃍𐃎𐃏𐃐𐃑𐃒𐃓𐃔𐃕𐃖𐃗𐃘𐃙𐃚𐃛𐃜𐃝𐃞𐃟𐃠𐃡𐃢𐃣𐃤𐃥𐃦𐃧𐃨𐃩𐃪𐃫𐃬𐃭𐃮𐃯𐃰𐃱𐃲𐃳𐃴𐃵𐃶𐃷𐃸𐃹𐃺𐃻𐃼𐃽𐃾𐃿𐄀𐄁𐄂𐄃𐄄𐄅𐄆𐄇𐄈𐄉𐄊𐄋𐄌𐄍𐄎𐄏𐄐𐄑𐄒𐄓𐄔𐄕𐄖𐄗𐄘𐄙𐄚𐄛𐄜𐄝𐄞𐄟𐄠𐄡𐄢𐄣𐄤𐄥𐄦𐄧𐄨𐄩𐄪𐄫𐄬𐄭𐄮𐄯𐄰𐄱𐄲𐄳𐄴𐄵𐄶𐄷𐄸𐄹𐄺𐄻𐄼𐄽𐄾𐄿𐅀𐅁𐅂𐅃𐅄𐅅𐅆𐅇𐅈𐅉𐅊𐅋𐅌𐅍𐅎𐅏𐅐𐅑𐅒𐅓𐅔𐅕𐅖𐅗𐅘𐅙𐅚𐅛𐅜𐅝𐅞𐅟𐅠𐅡𐅢𐅣𐅤𐅥𐅦𐅧𐅨𐅩𐅪𐅫𐅬𐅭𐅮𐅯𐅰𐅱𐅲𐅳𐅴𐅵𐅶𐅷𐅸𐅹𐅺𐅻𐅼𐅽𐅾𐅿𐆀𐆁𐆂𐆃𐆄𐆅𐆆𐆇𐆈𐆉𐆊𐆋𐆌𐆍𐆎𐆏𐆐𐆑𐆒𐆓𐆔𐆕𐆖𐆗𐆘𐆙𐆚𐆛𐆜𐆝𐆞𐆟𐆠𐆡𐆢𐆣𐆤𐆥𐆦𐆧𐆨𐆩𐆪𐆫𐆬𐆭𐆮𐆯𐆰𐆱𐆲𐆳𐆴𐆵𐆶𐆷𐆸𐆹𐆺𐆻𐆼𐆽𐆾𐆿𐇀𐇁𐇂𐇃𐇄𐇅𐇆𐇇𐇈𐇉𐇊𐇋𐇌𐇍𐇎𐇏𐇐𐇑𐇒𐇓𐇔𐇕𐇖𐇗𐇘𐇙𐇚𐇛𐇜𐇝𐇞𐇟𐇠𐇡𐇢𐇣𐇤𐇥𐇦𐇧𐇨𐇩𐇪𐇫𐇬𐇭𐇮𐇯𐇰𐇱𐇲𐇳𐇴𐇵𐇶𐇷𐇸𐇹𐇺𐇻𐇼𐇽𐇾𐇿𐈀𐈁𐈂𐈃𐈄𐈅𐈆𐈇𐈈𐈉𐈊𐈋𐈌𐈍𐈎𐈏𐈐𐈑𐈒𐈓𐈔𐈕𐈖𐈗𐈘𐈙𐈚𐈛𐈜𐈝𐈞𐈟𐈠𐈡𐈢𐈣𐈤𐈥𐈦𐈧𐈨𐈩𐈪𐈫𐈬𐈭𐈮𐈯𐈰𐈱𐈲𐈳𐈴𐈵𐈶𐈷𐈸𐈹𐈺𐈻𐈼𐈽𐈾𐈿𐉀𐉁𐉂𐉃𐉄𐉅𐉆𐉇𐉈𐉉𐉊𐉋𐉌𐉍𐉎𐉏𐉐𐉑𐉒𐉓𐉔𐉕𐉖𐉗𐉘𐉙𐉚𐉛𐉜𐉝𐉞𐉟𐉠𐉡𐉢𐉣𐉤𐉥𐉦𐉧𐉨𐉩𐉪𐉫𐉬𐉭𐉮𐉯𐉰𐉱𐉲𐉳𐉴𐉵𐉶𐉷𐉸𐉹𐉺𐉻𐉼𐉽𐉾𐉿𐊀𐊁𐊂𐊃𐊄𐊅𐊆𐊇𐊈𐊉𐊊𐊋𐊌𐊍𐊎𐊏𐊐𐊑𐊒𐊓𐊔𐊕𐊖𐊗𐊘𐊙𐊚𐊛𐊜𐊝𐊞𐊟𐊠𐊡𐊢𐊣𐊤𐊥𐊦𐊧𐊨𐊩𐊪𐊫𐊬𐊭𐊮𐊯𐊰𐊱𐊲𐊳𐊴𐊵𐊶𐊷𐊸𐊹𐊺𐊻𐊼𐊽𐊾𐊿𐋀𐋁𐋂𐋃𐋄𐋅𐋆𐋇𐋈𐋉𐋊𐋋𐋌𐋍𐋎𐋏𐋐𐋑𐋒𐋓𐋔𐋕𐋖𐋗𐋘𐋙𐋚𐋛𐋜𐋝𐋞𐋟𐋠𐋡𐋢𐋣𐋤𐋥𐋦𐋧𐋨𐋩𐋪𐋫𐋬𐋭𐋮𐋯𐋰𐋱𐋲𐋳𐋴𐋵𐋶𐋷𐋸𐋹𐋺𐋻𐋼𐋽𐋾𐋿𐌀𐌁𐌂𐌃𐌄𐌅𐌆𐌇𐌈𐌉𐌊𐌋𐌌𐌍𐌎𐌏𐌐𐌑𐌒𐌓𐌔𐌕𐌖𐌗𐌘𐌙𐌚𐌛𐌜𐌝𐌞𐌟𐌠𐌡𐌢𐌣𐌤𐌥𐌦𐌧𐌨𐌩𐌪𐌫𐌬𐌭𐌮𐌯𐌰𐌱𐌲𐌳𐌴𐌵𐌶𐌷𐌸𐌹𐌺𐌻𐌼𐌽𐌾𐌿𐍀𐍁𐍂𐍃𐍄𐍅𐍆𐍇𐍈𐍉𐍊𐍋𐍌𐍍𐍎𐍏𐍐𐍑𐍒𐍓𐍔𐍕𐍖𐍗𐍘𐍙𐍚𐍛𐍜𐍝𐍞𐍟𐍠𐍡𐍢𐍣𐍤𐍥𐍦𐍧𐍨𐍩𐍪𐍫𐍬𐍭𐍮𐍯𐍰𐍱𐍲𐍳𐍴𐍵𐍶𐍷𐍸𐍹𐍺𐍻𐍼𐍽𐍾𐍿𐎀𐎁𐎂𐎃𐎄𐎅𐎆𐎇𐎈𐎉𐎊𐎋𐎌𐎍𐎎𐎏𐎐𐎑𐎒𐎓𐎔𐎕𐎖𐎗𐎘𐎙𐎚𐎛𐎜𐎝𐎞𐎟𐎠𐎡𐎢𐎣𐎤𐎥𐎦𐎧𐎨𐎩𐎪𐎫𐎬𐎭𐎮𐎯𐎰𐎱𐎲𐎳𐎴𐎵𐎶𐎷𐎸𐎹𐎺𐎻𐎼𐎽𐎾𐎿𐏀𐏁𐏂𐏃𐏄𐏅𐏆𐏇𐏈𐏉𐏊𐏋𐏌𐏍𐏎𐏏𐏐𐏑𐏒𐏓𐏔𐏕𐏖𐏗𐏘𐏙𐏚𐏛𐏜𐏝𐏞𐏟𐏠𐏡𐏢𐏣𐏤𐏥𐏦𐏧𐏨𐏩𐏪𐏫𐏬𐏭𐏮𐏯𐏰𐏱𐏲𐏳𐏴𐏵𐏶𐏷𐏸𐏹𐏺𐏻𐏼𐏽𐏾𐏿𐐀𐐁𐐂𐐃𐐄𐐅𐐆𐐇𐐈𐐉𐐊𐐋𐐌𐐍

43,4

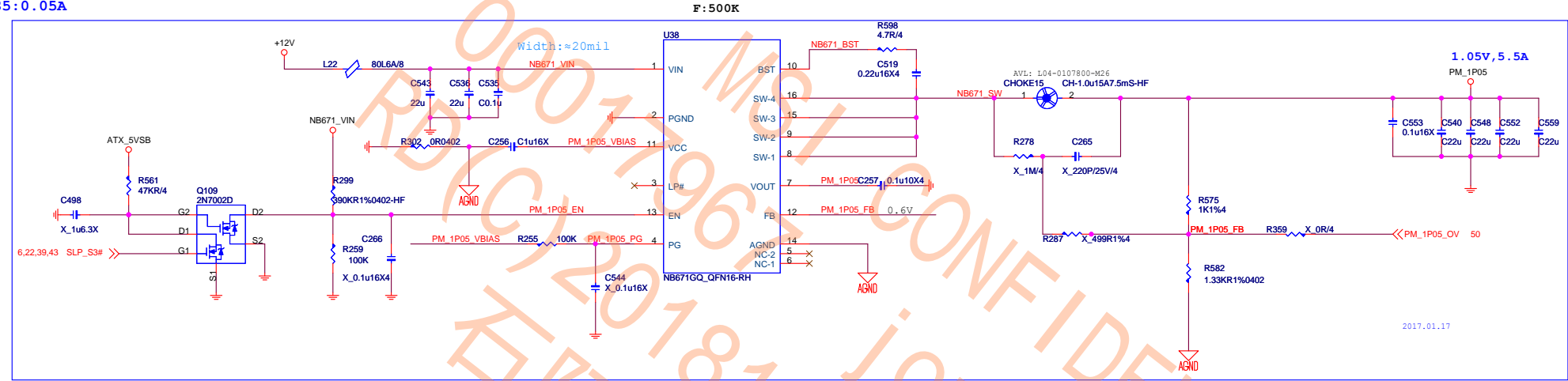
FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

support OV=>NB685
not support OV=> NB681

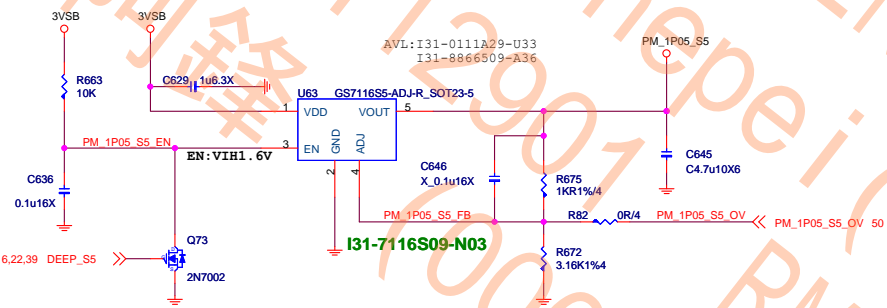
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH≤L≤1.1664uH



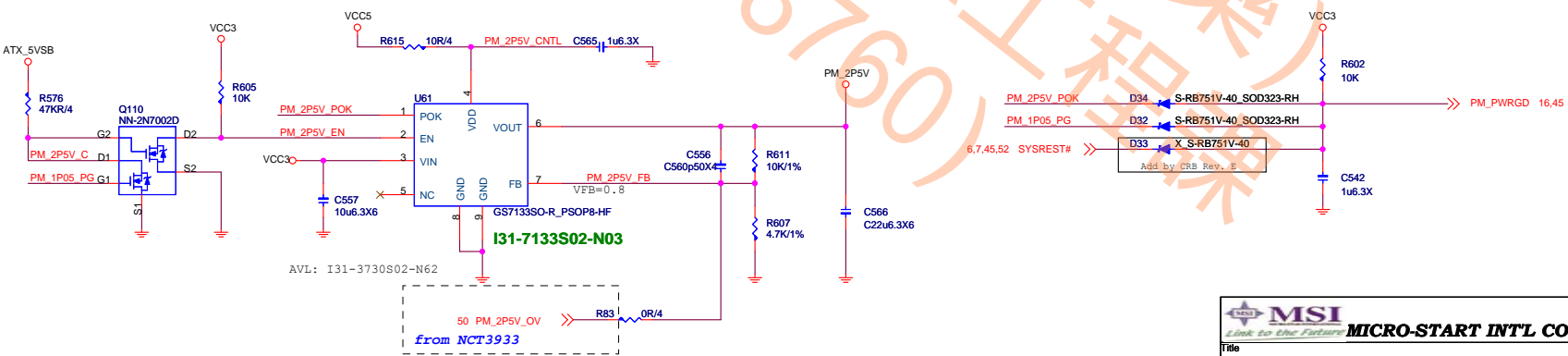
FOR Promontory 1.05V_S5

0.05A

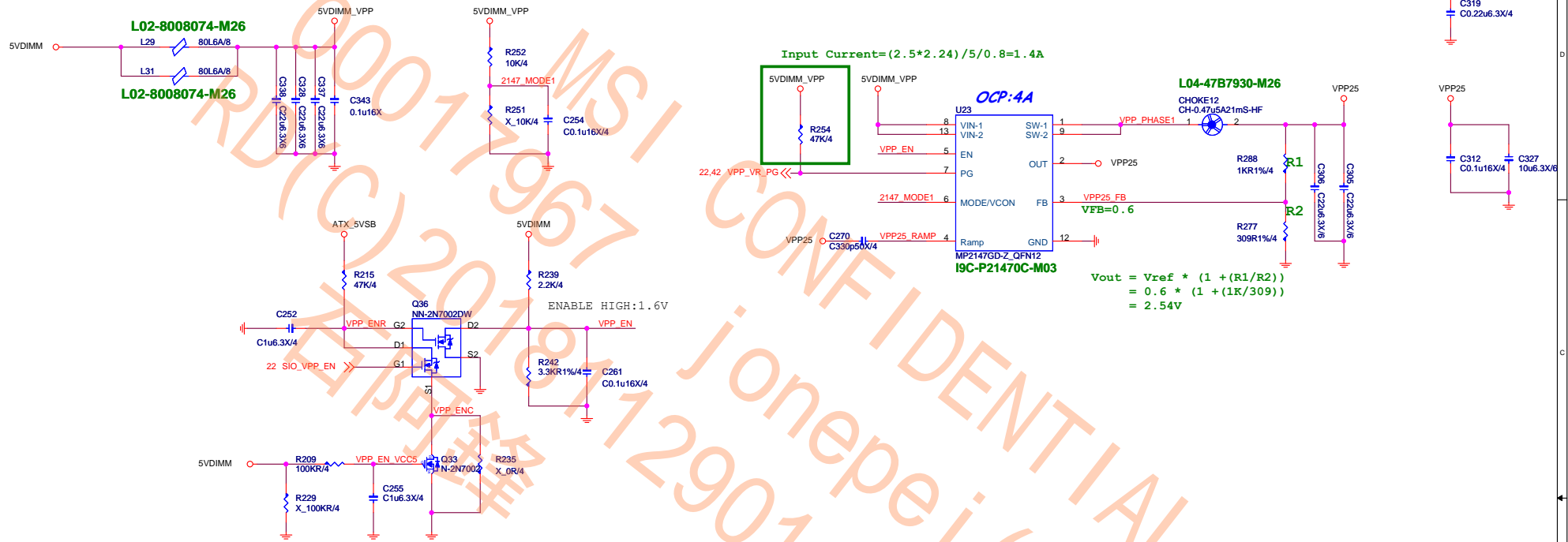


Promontory-2.5V

2.5V; 900mA

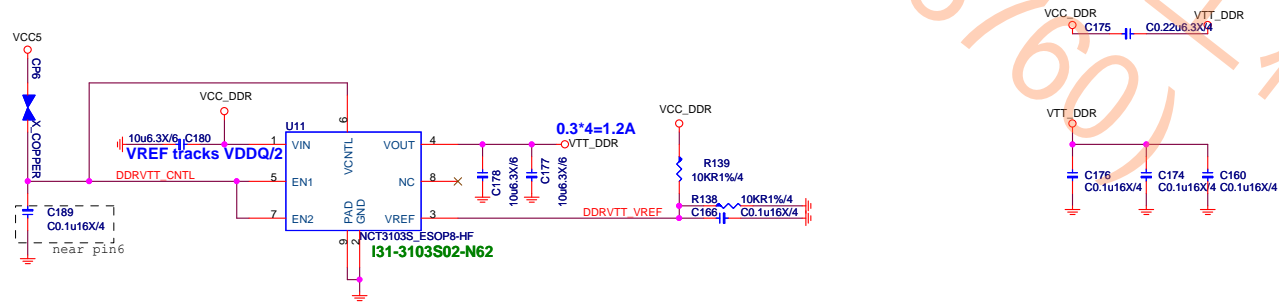


2.5V@2.24A

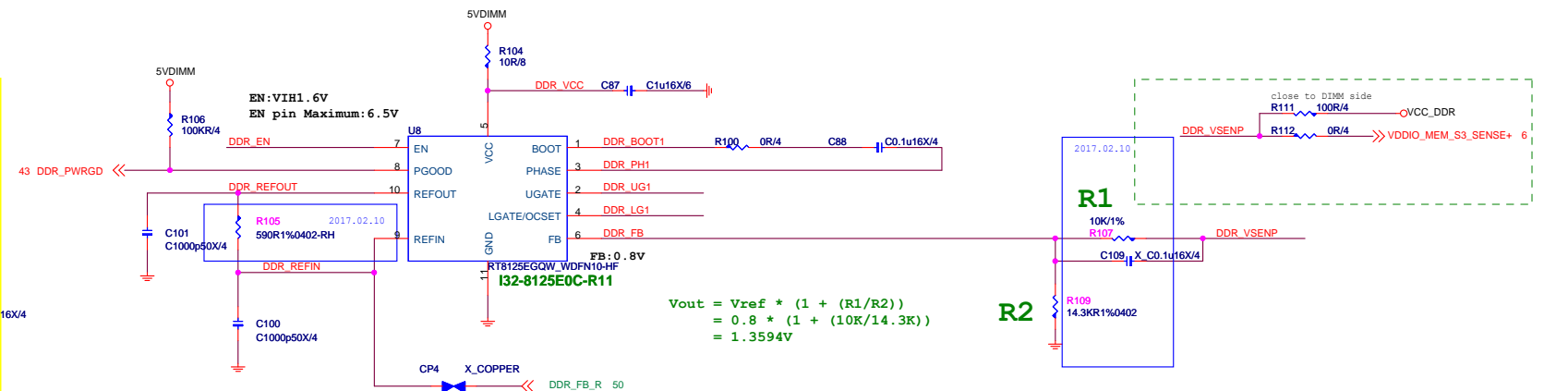
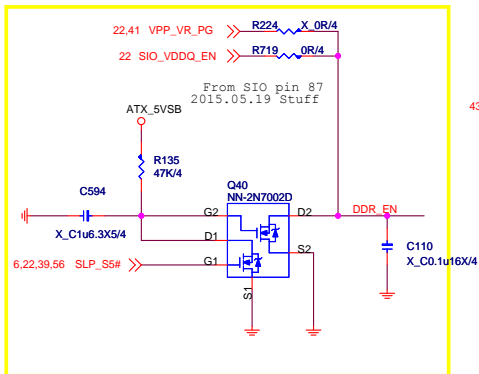


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

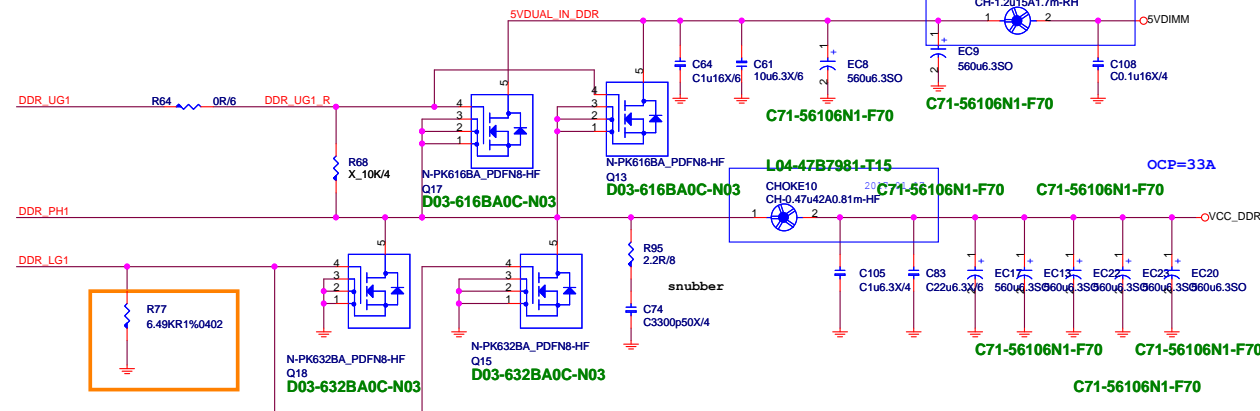
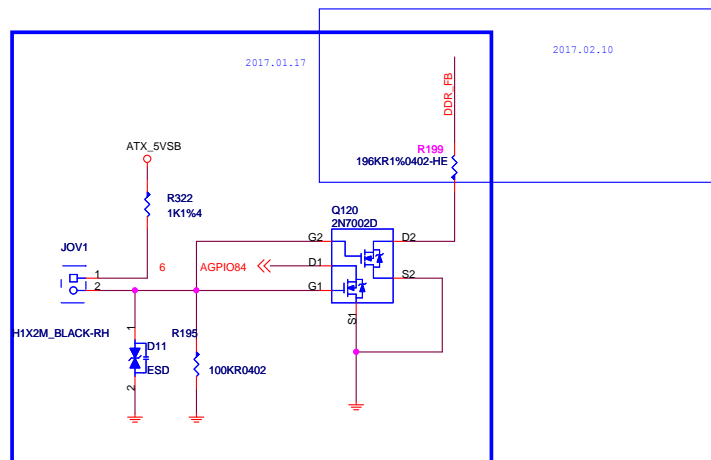


15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT



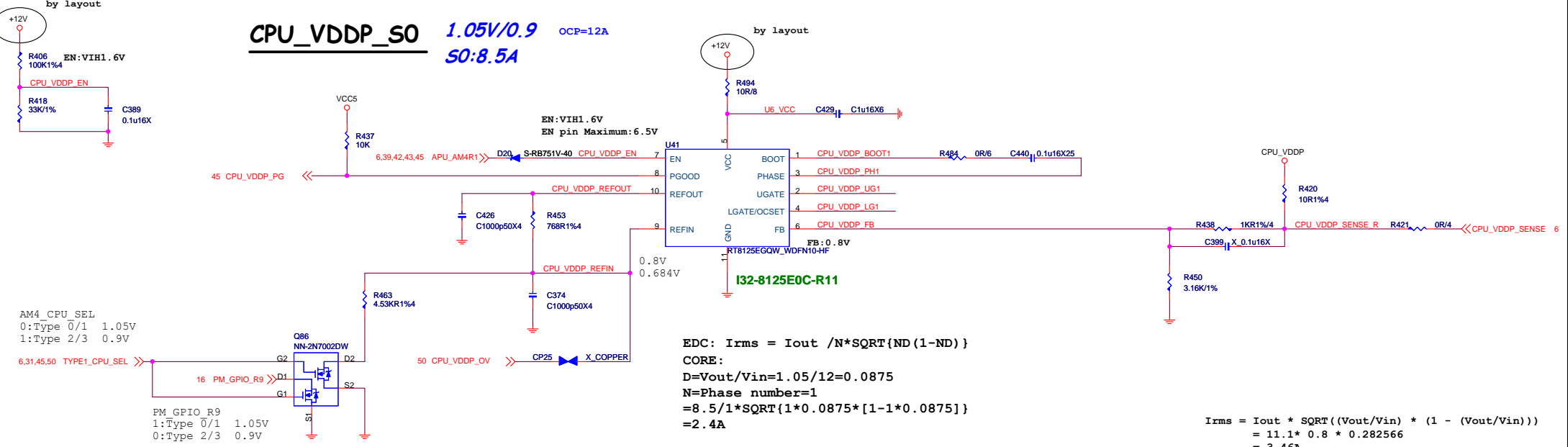
EN:VIH2V
EN pin Maximum:5.5V,RECOMMENDED:3.6V

EDC: $I_{rms} = I_{out} / N \cdot \sqrt{ND(1-ND)}$
 CORE:
 $D = V_{out} / V_{in} = 1.2 / 5 = 0.24$
 $N = \text{Phase number} = 1$
 $= 26.2 / 1 \cdot \sqrt{0.24 \cdot [1 - 0.24]}$
 $= 11.189A$

$$\begin{aligned} OCP &= 26.2A * 1.5 = 39.3A \\ R_{ocs}(R95) &= OCP * R_{dson}[Low\ side] / 10uA \\ &= 35A * 1.65mohm / 10uA \\ &= 5.77K \end{aligned}$$


CPU_VDDP_S0

1.05V/0.9
S0:8.5A



TYPE0_CPU_SEL:
1:Type 0
0:Type 2

CPU_VDDP_EN:
0:Type 2
1:Type 0

6.45 TYPE0_CPU_SEL

VDDP_SEL

6.31,45,50 TYPE1_CPU_SEL

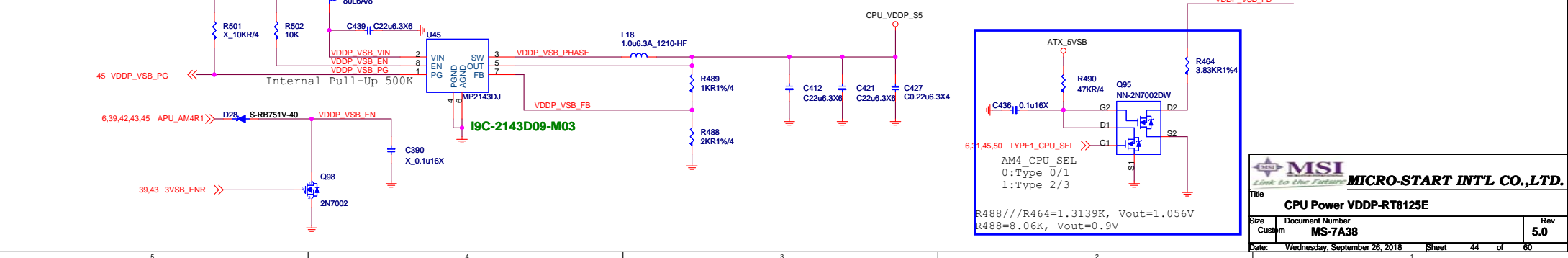
TYPE1_CPU_SEL:
0:Type 0
1:Type 2

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

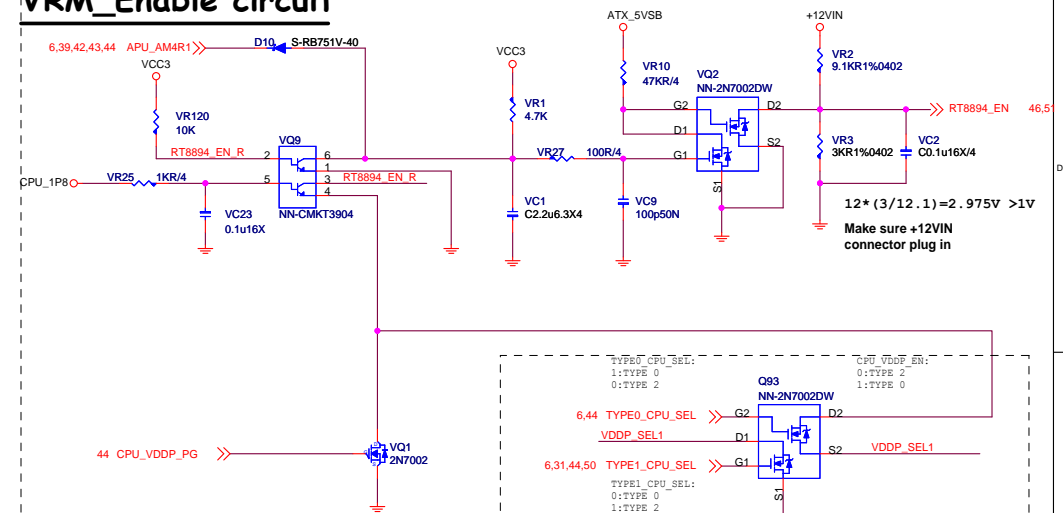
CPU_VDDP NOT SUPPORT TYPE2

CPU_VDDP_S5

VDDP_S5 1.05V/0.9
S5:1A



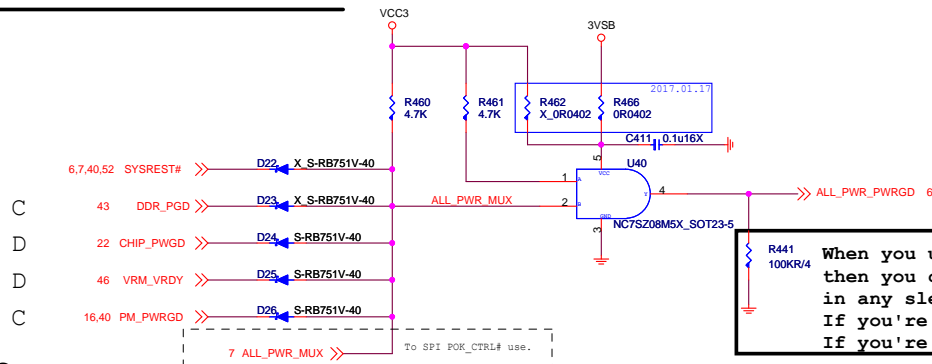
VRM_Enable circuit



CPU VDDP NOT SUPPORT TYPE2

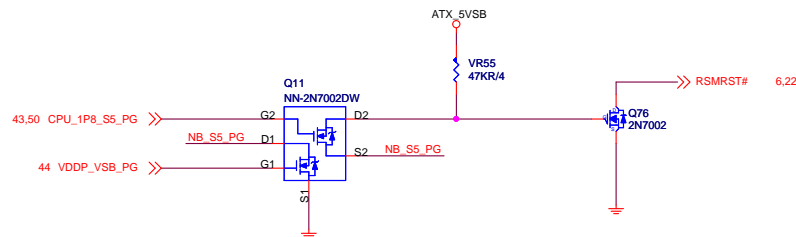
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

ALL POWER GOOD MUX

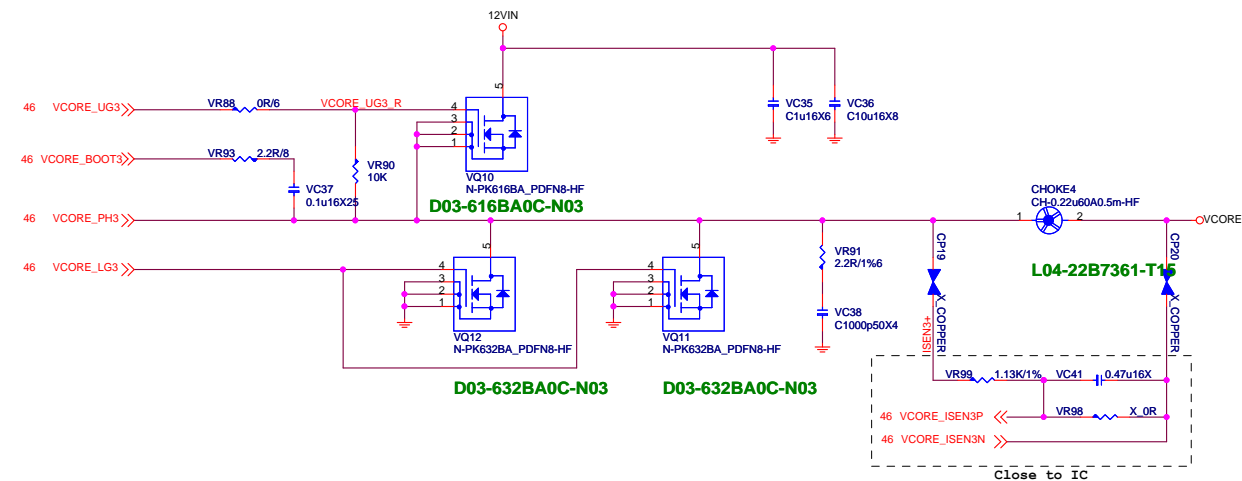
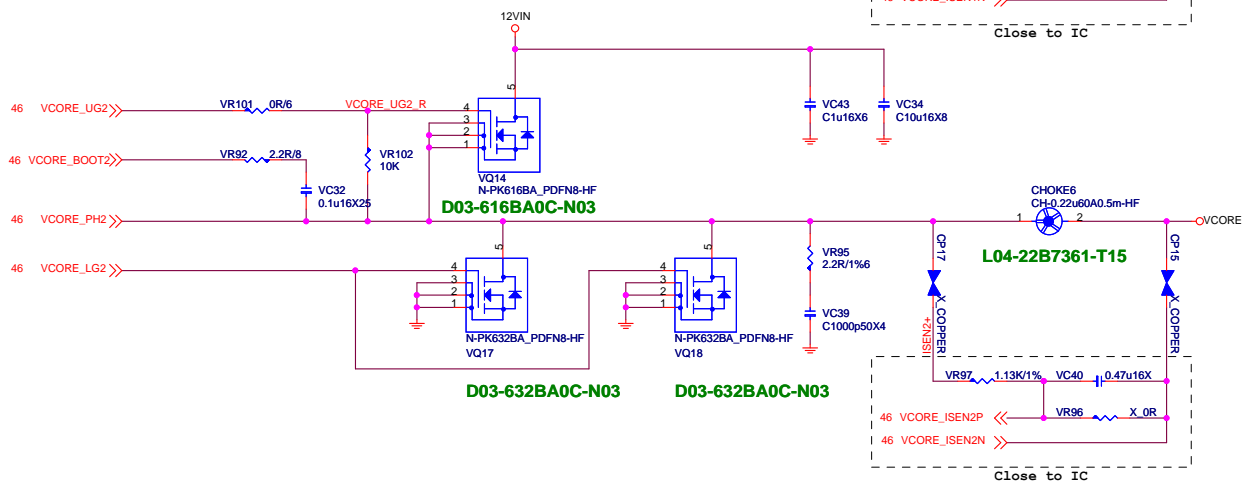
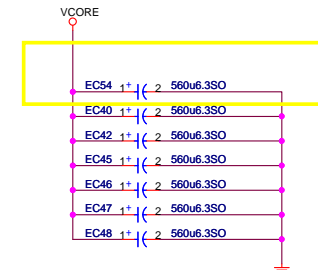
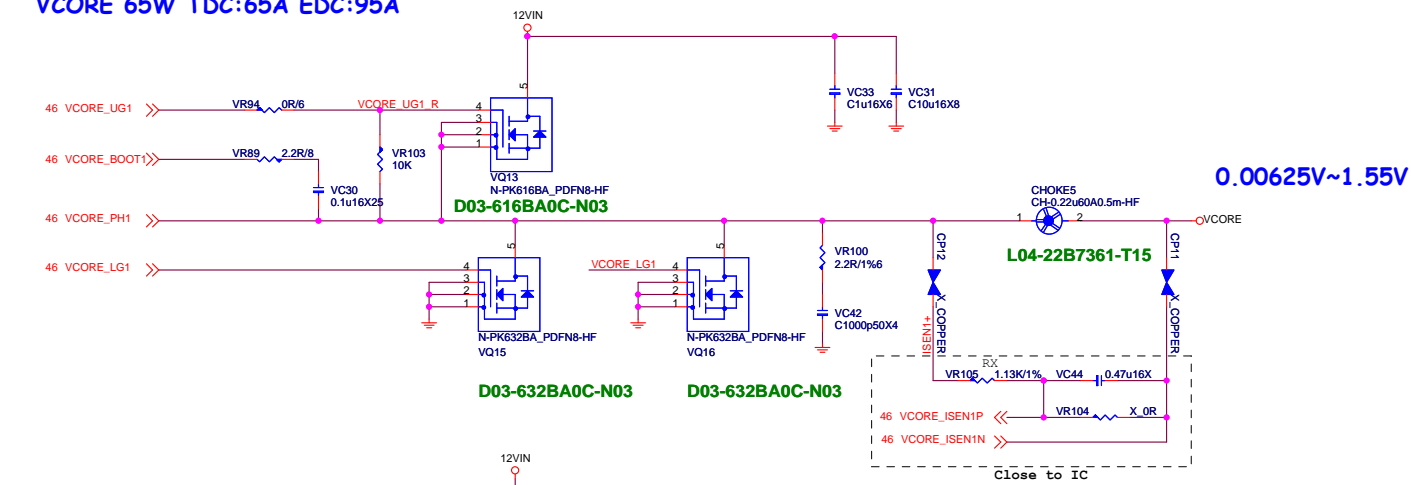


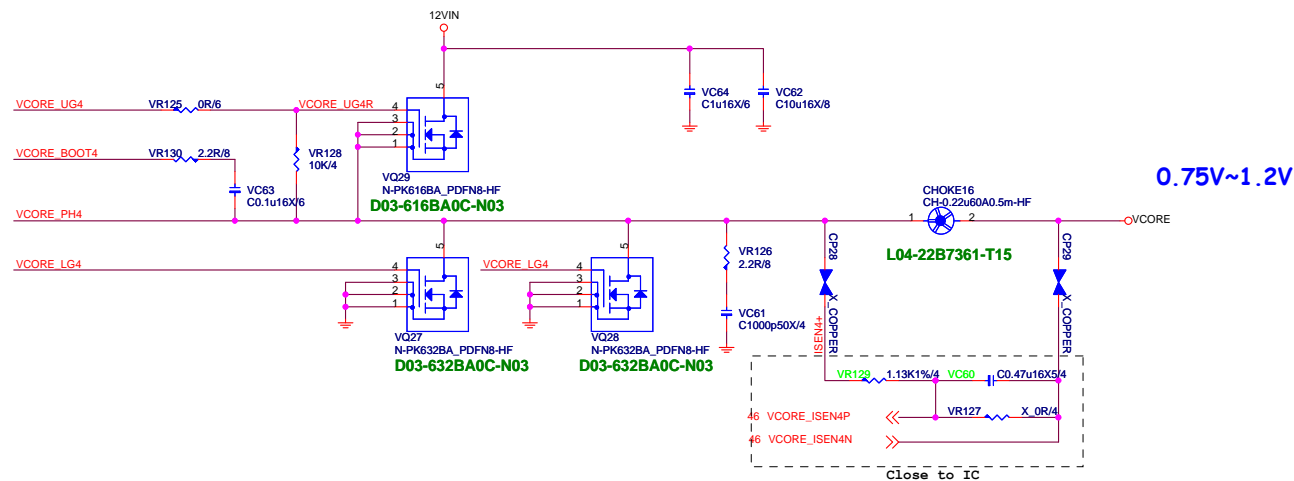
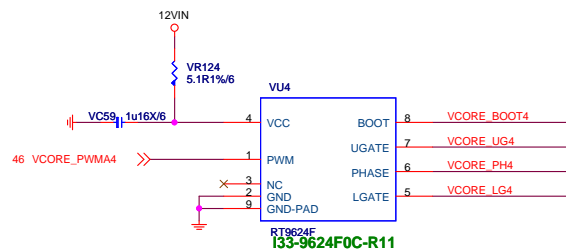
S0 PG

S5 PG

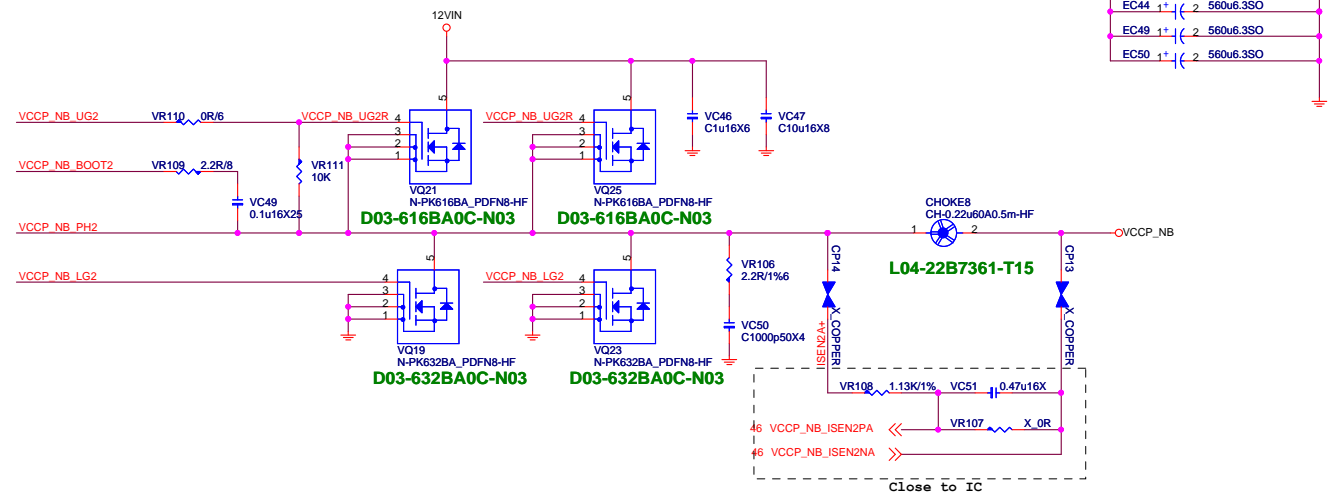
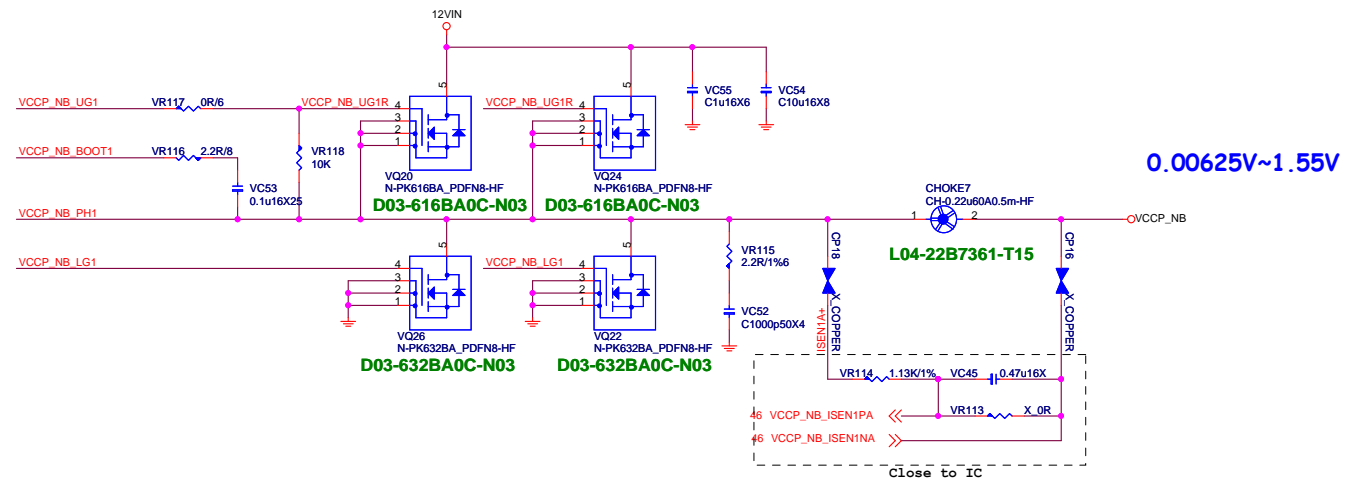
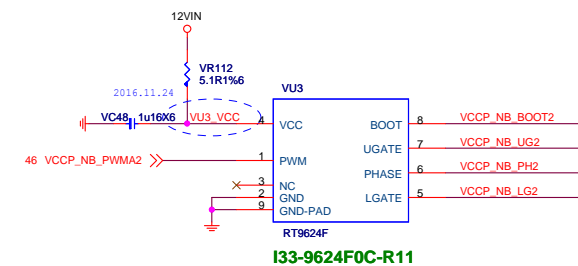
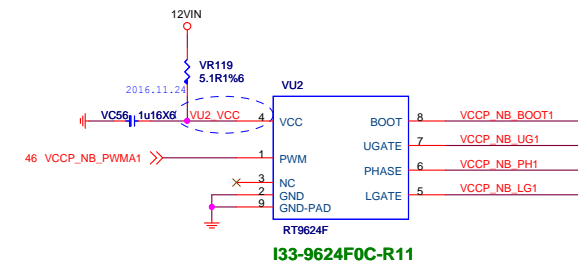


VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A





VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

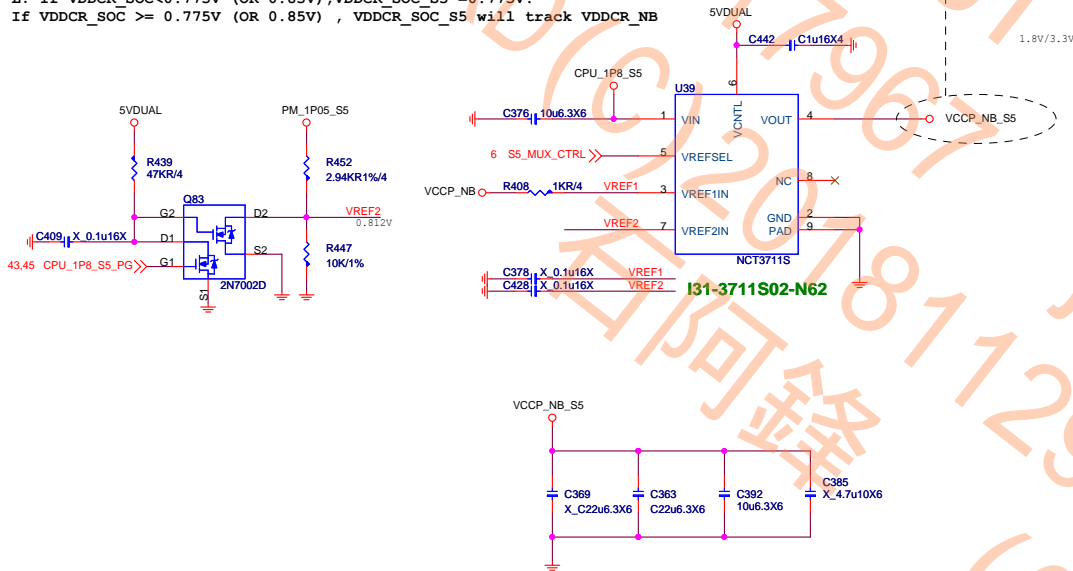


FOR VCCP_SOC_S5
0.9A

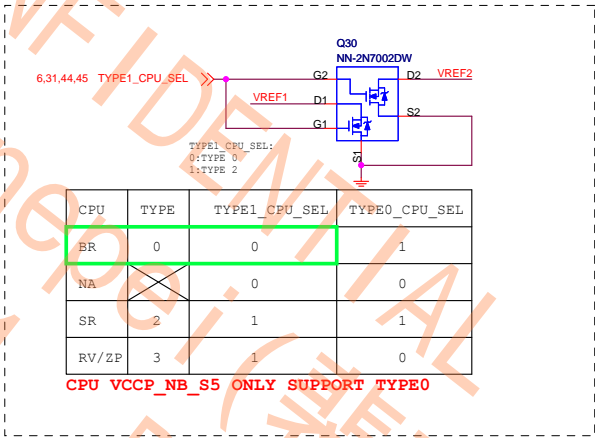
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

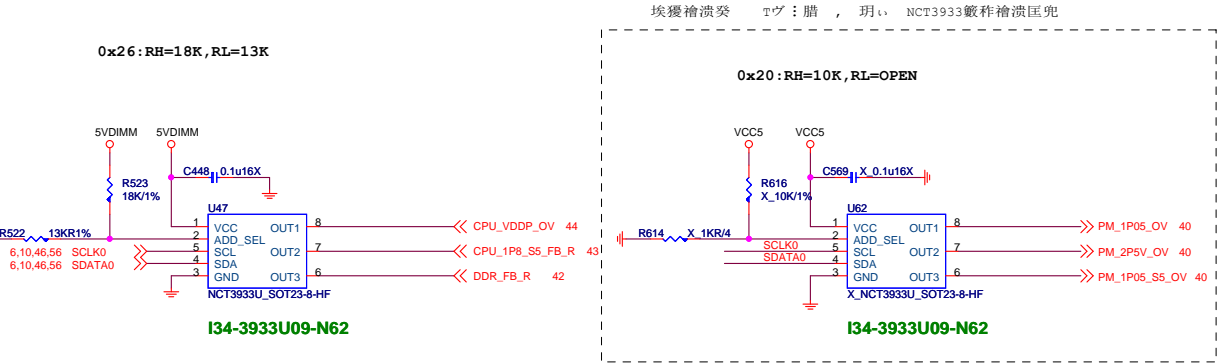
H: +VDDCR_FCH ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB



(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0

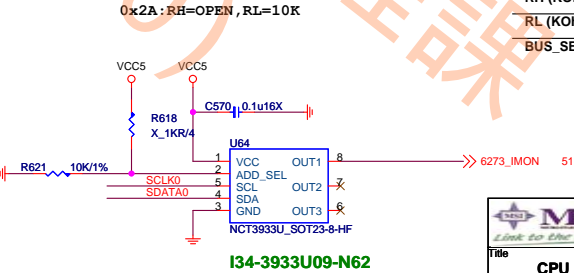



Over Voltage Control IC



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



**MICRO-START INTL CO.,LTD.**

File
CPU Power NB Switch/NCT3933

Size
Custom

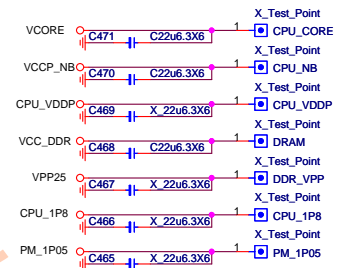
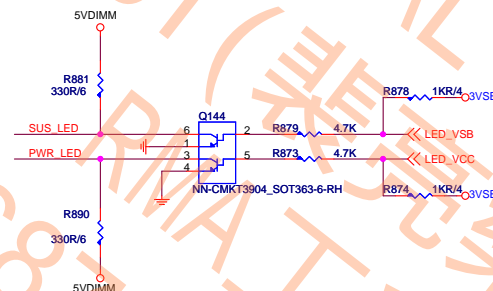
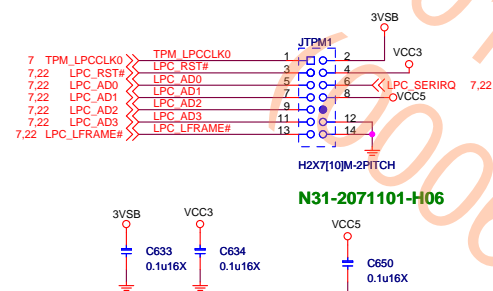
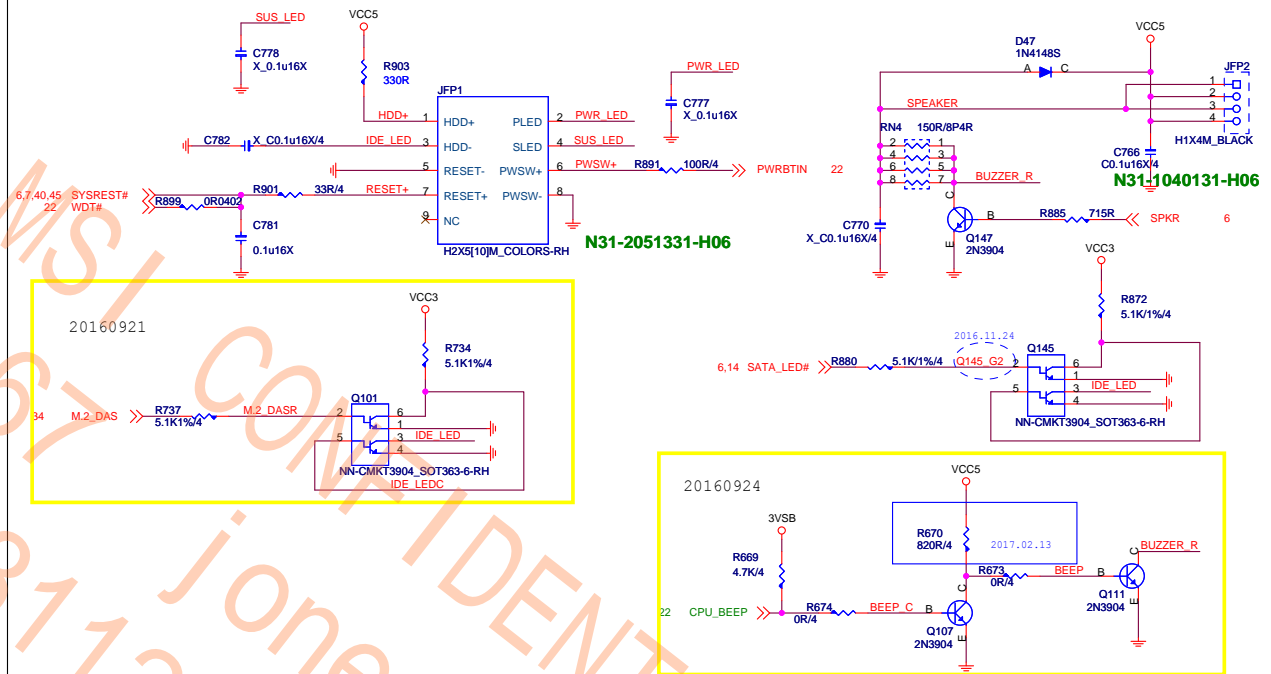
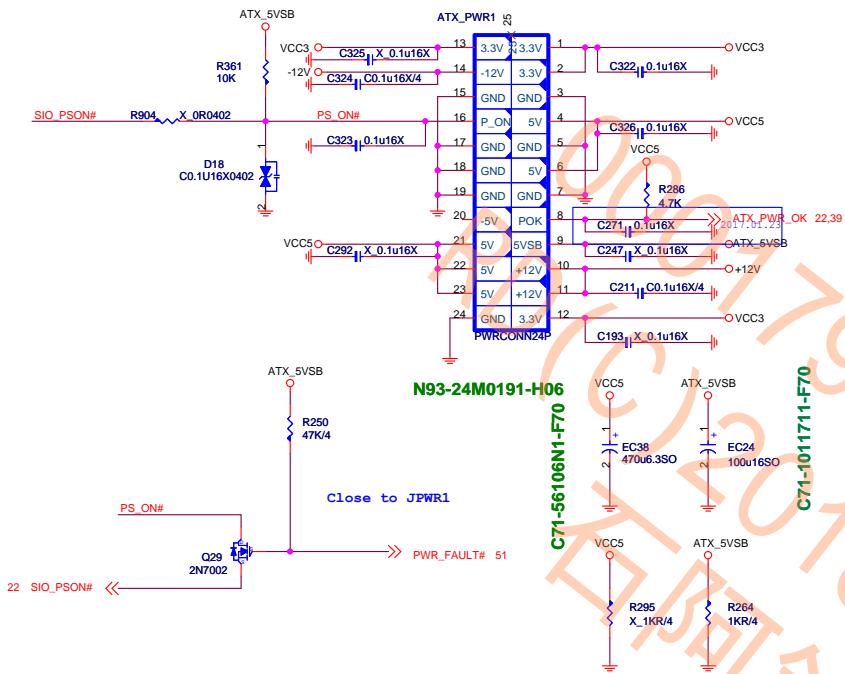
Document Number
MS-7A38

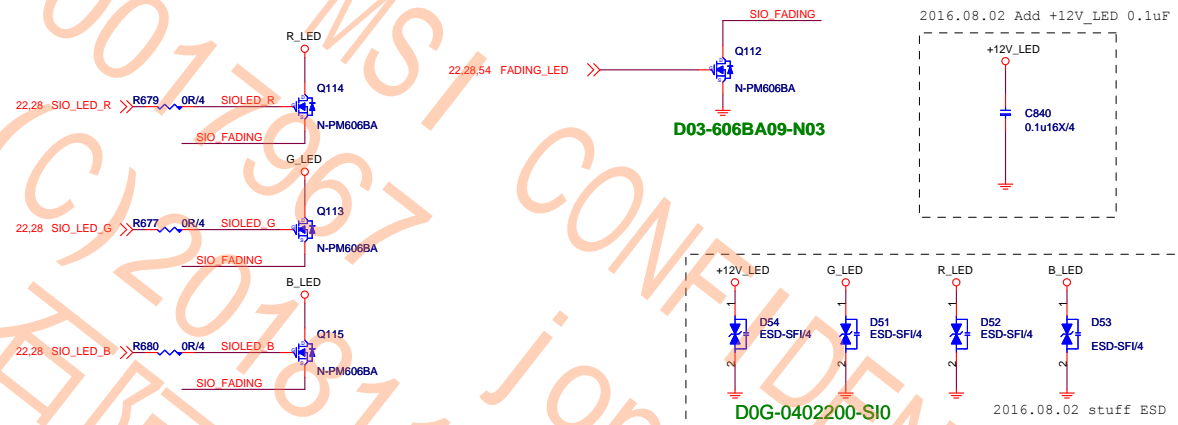
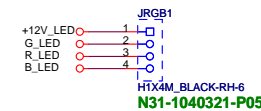
Date
Wednesday, September 26, 2018

Sheet
50

Rev
5.0

of
60

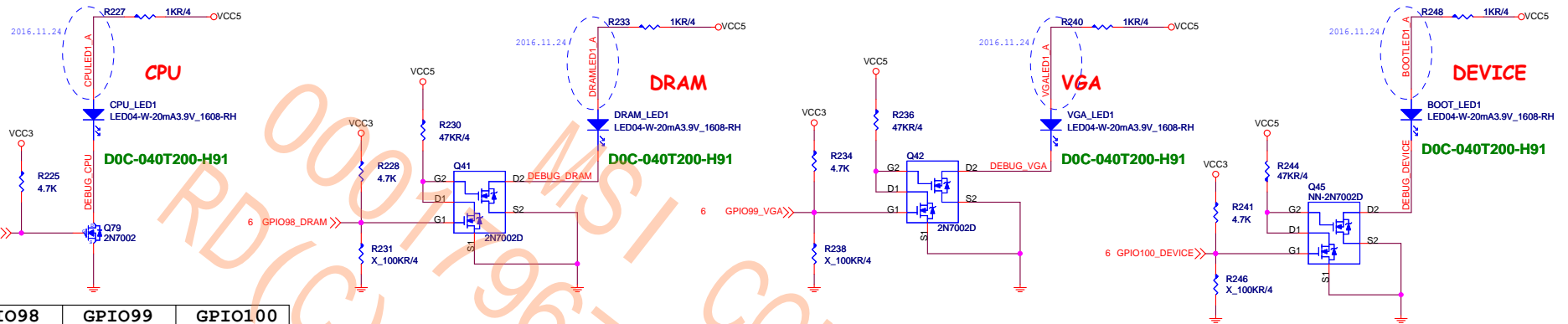




FCH LED Place under Heat-sink

LED
翺 : D0C-040S600-E07
フ : D0C-040S300-E07

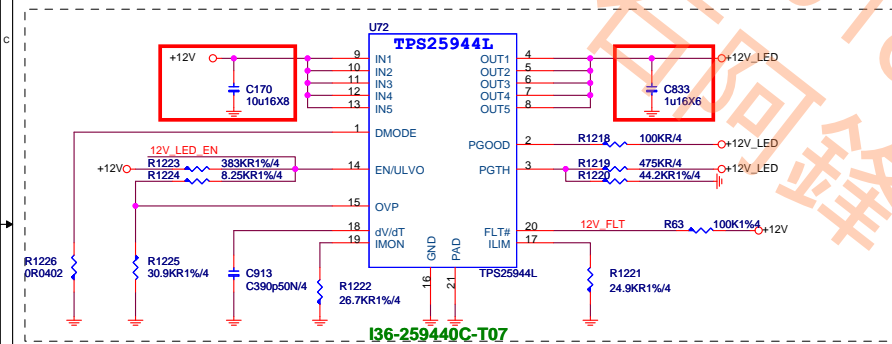
EZ Debug LED



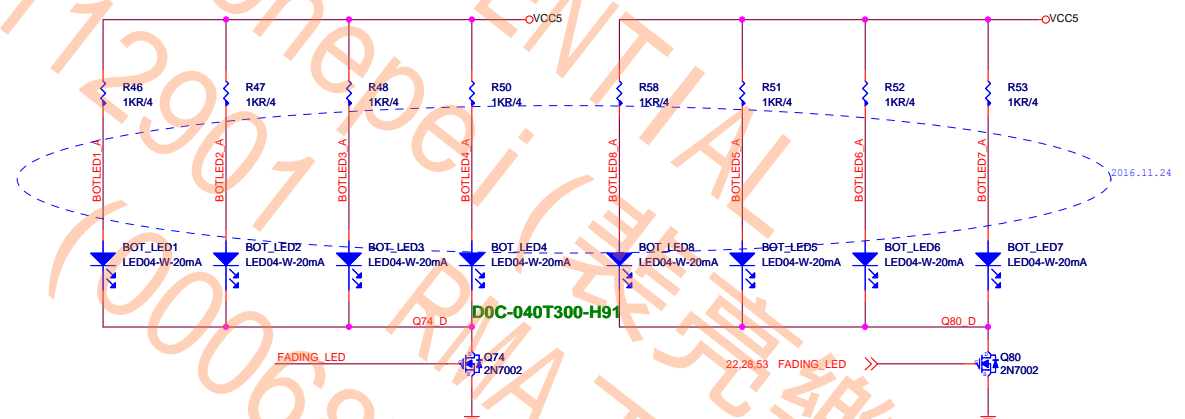
GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獠	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED Control by SIO

2016.07.06 Use TPS25944L

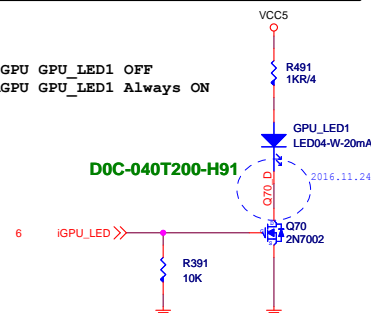


Bottom LED

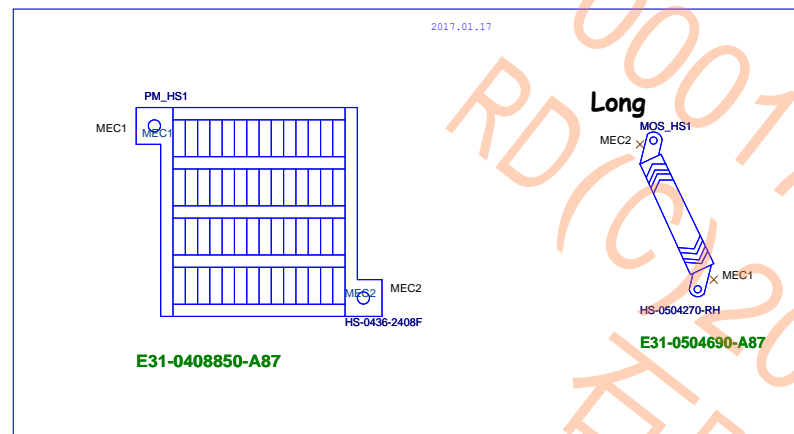


AM4 APU Detect LED Circuit

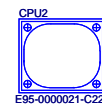
```
iGPU GPU_LED1 OFF
dGPU GPU_LED1 Always ON
```



HEAT SINK

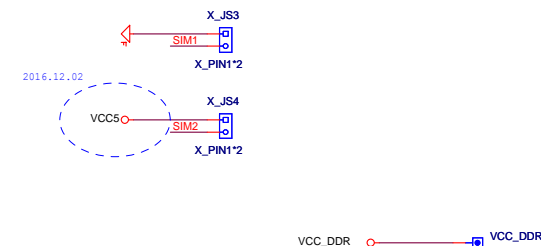


CPU Socket

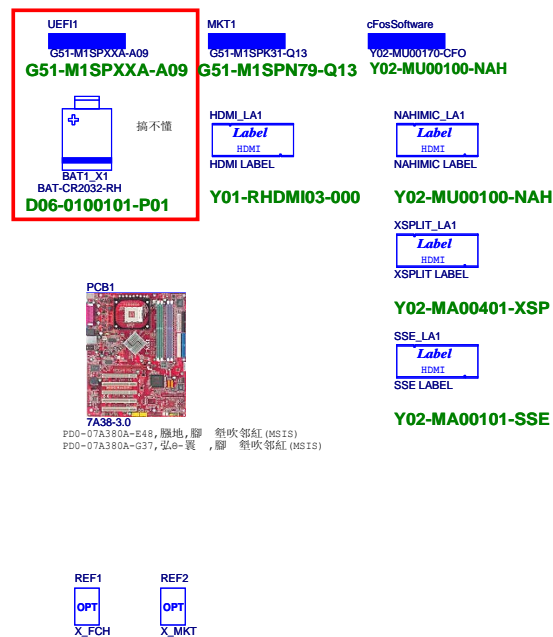


RETENTION MODULE
E95-000022-C22

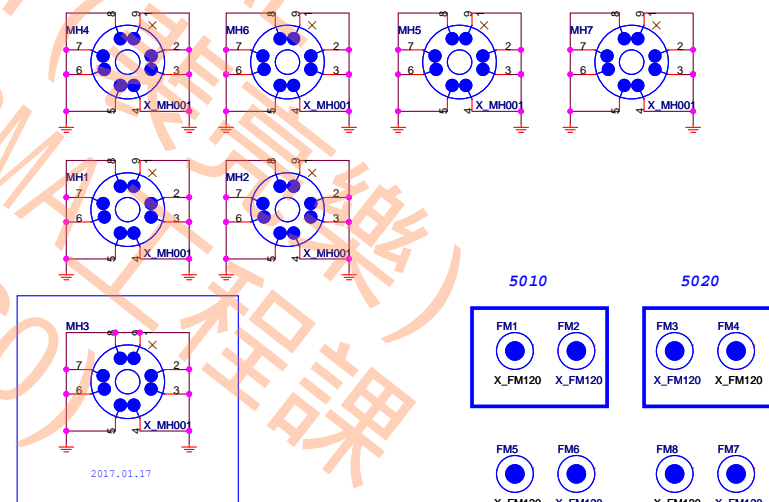
Simulation




MANUAL PART



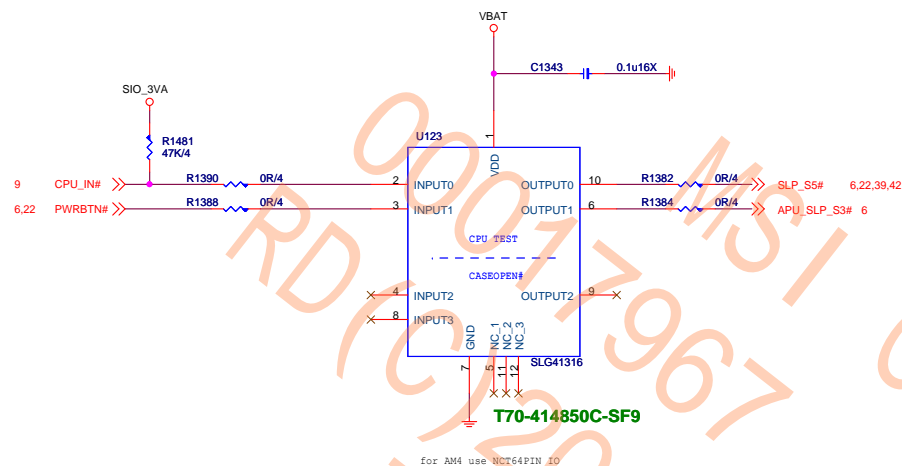
Optics Orientation Holes



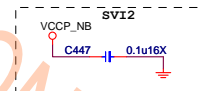
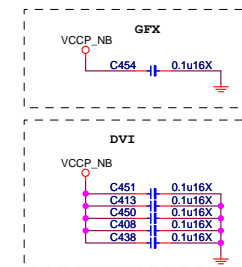
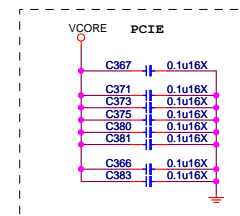
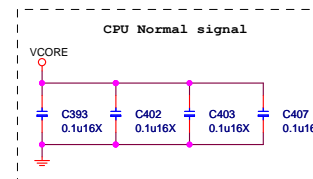
OPT	Configure	BOM	Function
		601-7A38-A01	XXXX


MSI
 Link to the Future
MICRO-START INT'L CO.,LTD.

Title	
BOM Option	
Size Document Number	Rev
Custom MS-7A38	5.0
Date: Wednesday, September 26, 2018	Sheet 55 of 60



Moat Cap



RTC & Clear CMOS Circuit

